Journal of Harbin Engineering University ISSN: 1006-7043

Vol 44 No. 8
August 2023

Review on Switched Capacitor Multilevel Inverter

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Abstract— The switched capacitor multilevel inverter (SCMI) is a viable alternative to traditional multilevel inverters due to its ability to handle higher power and voltage levels. The switched capacitor multilevel inverter is examined in depth in this work. Control techniques used in SCMI systems, such as voltage balancing, capacitor voltage regulation, and output waveform creation, are also investigated. The importance of precise control in obtaining peak performance and dependable operation is emphasised, and contemporary developments in control methods are covered.

The output waveform quality and overall system efficiency are both heavily influenced by the modulation technique used. This paper synthesises the present state of switched capacitor multilevel inverter research and development, with an eye on the inverters' potential to alter the status quo of high-power, high-voltage uses. The use of multilevel inverters has become commonplace in renewable energy systems. In addition to lowering the size of the filter and simplifying the circuitry, these inverters' output voltages are more sinusoidal and have less harmonics than those of traditional two-level inverters. When the number of output voltage levels is increased in traditional multilevel inverter topologies, the resulting circuitry becomes cumbersome and expensive. In this study, we provide a comprehensive review of the recently developed SCMLIs. The various SCMLIs have been sorted into groups according to their voltage gains and amount of complexity. In this study, we present a comprehensive contrast.

Keywords— *Cascaded H-bridge, multilevel inverter (MLI), pulse width modulation (PWM) Multi-Level Inverter, PWM, Switching Functions.*

Introduction

Power electronics have come a long way in recent years due to the increasing need for high-efficiency, high-power, and high-voltage solutions for power conversion. The constraints of voltage and power management have led to the development of multilevel inverters as a viable alternative to conventional two-level inverters. The Switched Capacitor Multilevel Inverter (SCMI) is one of the most talked-about of these new multilevel topologies because of

its novel method of producing many voltage levels at once.Inverters are used in a wide variety of electric motors, renewable energy systems, and grid-connected applications because of their ability to convert direct current (DC) to alternating current (AC). Traditional two-level inverters have low efficiency and large switching losses in high-power and high-voltage applications because of their poor voltage and power management. By synthesising several voltage levels, multilevel inverters are able to overcome these constraints and increase power quality by lowering harmonic distortion and enhancing voltage waveforms.

Because of its unique implementation of switched capacitors to create multilayer voltage outputs, the SCMI stands out among multilevel inverters. In order to redistribute energy and create numerous voltage levels, SCMI uses a mix of capacitors and switches, as opposed to the large number of power semiconductor switches and voltage sources required by conventional multilevel inverters. Reduced component count, lower switching losses, higher voltage levels, better voltage balancing, and increased efficiency are just a few of the benefits of this novel technique. The goal of this research is to give a grounding knowledge of SCMI technology, a revolutionary inverter architecture with the potential

to revolutionise high-power and high-voltage conversion systems. The SCMI provides a compelling outlet for academics and practitioners to investigate and push the limits of power electronics technology, which is increasingly in demand as the need for more efficient and diverse power electronic solutions grows.

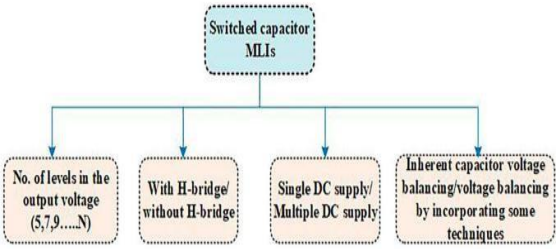


Figure: 1 Categorization of switched-capacitor MLIs

The limitations of traditional energy sources, such as their scarcity and environmental impact, necessitate exploration of other strategies. In an effort to reduce greenhouse gas emissions, investments in people and technology have turned towards renewable resources. The rapid use of solar and wind power, for example, is largely attributable to advancements in power electronics. Much research has gone into the various converters that may be utilised to connect these resources to the grid or meet the demand of local loads. Multilevel inverters are a typical form of converter that may provide an appropriate alternating supply from a direct current source. Sinusoidal ac voltage may be generated from many dc voltage sources using multilevel inverters. Diode clamped, capacitor clamped, and cascaded H-bridge are the three most frequent multilevel inverter topologies. Industrial uses of conventional MLIs, such as the diode-clamped architecture and the flying capacitor topology, are confined to low-voltage applications because to the enormous number of components required for high-voltage production. The uneven voltage across series-connected capacitors is another key shortcoming of these topologies. The primary disadvantage of the cascaded H-bridge architecture (Figure 1) is the requirement for a large number of individual dc sources. Transform-based topologies and the quasi-Z-source approach are only two examples of the newer topologies that have been created in recent years to overcome the limitations of conventional multilevel inverters. Multilayer inverters (MLIs) use a series-parallel configuration that has gained popularity in recent years. There is a lot of stress from the accumulated voltage on the H-bridge multilevel inverters at the back of the system. Research is done on several topologies that use fewer physically distinct dc sources, power switches, diodes, and capacitors to produce a smaller footprint with lower losses, lower total standing voltage, and lower cost. The suggested structures are often modular and adaptable in design, allowing for a wide range of voltage levels to be offered in order to enhance and approach the sinusoidal output voltage for medium- and high-power applications like electric motors, solar PV integrated systems, and so on. Current multilevel inverters do not have the capacity to boost voltage. In order to work with grid-connected systems, converters designed for PV and fuel cell systems will need to boost the voltage their source devices produce. For instance, voltage boost is a feature of several topologies. Voltage may be increased by 1.52025 or 3.2632 with seven-level MLIs. Voltage gains of 233–35 and 4.36–44 volts are possible from SCMLIs with nine output voltage levels. In the following paragraphs, we will discuss SCMLIs, which have the natural ability to raise voltage. Since some MLI topologies only achieve a small voltage gain despite using many power switches and isolated dc sources, switched capacitor multilevel inverters have received a great deal of attention as a potentially useful small module with voltage boosting capability while using the fewest possible dc sources.

1. Literature Review

Chettiar Ramachandra et. All (2019) Single-phase asymmetrical multilevel inverters are shown with a novel architecture based on SCISPC. The inverter consists of a H bridge inverter and a level generator. It was determined that a multi carrier PWM would be the most effective method of achieving the necessary effects while also decreasing harmonics and switching losses. A switching capacitor based series parallel control was also used to achieve higher voltage levels with fewer DC sources. This research analysed the results of simulations and experiments in great detail. To test the efficacy of this method, a hardware prototype was constructed utilising a DSPIC controller to generate the switching pulse's at fixed angles. [1]

Mohammad Tayyab et. All (2021) Using one bidirectional switch, ten unidirectional switches, one DC source, three diodes, and three capacitors, a 13-level switched-capacitor multilevel inverter (MLI) is proposed and analysed in this study. Because of its inherent self-voltage balancing capabilities, the proposed MLI doesn't need a complex control circuit for balancing capacitor voltage. In-depth MATLAB simulations and analyses of the proposed 13-level converter's performance are presented. The performance of the proposed MLI is experimentally validated with R and RL loads using the prototype developed in the lab, and we find that it performs adequately in both cases. The load changes and modulation index (M) are part of the battery of testing. The TSV of the proposed converter is quite low, coming in at just 22. The proposed converter increases efficiency by a factor of three, uses fewer switches, and has a lower TSV. The total harmonic distortion (THD) of the recommended inverter's output voltage is 4.9%, which is well within IEEE-519 guidelines. Efficiency peaks at 97.2 percent with a 200-watt load. [2]

Saifullah Kakar et. All (2021) An original switched-capacitor MLI (SC-MLI) is introduced here. Using the inverter, the voltage of switched capacitors may be automatically balanced, and the voltage can be increased by a factor of three. We have covered what switched capacitors are, how they work, and the several ways they may be used, including their charging and discharging cycles. The proposed SC-MLI takes a single input and outputs a voltage waveform with 13 different levels. Additionally, they discovered that voltage strain at power switches was tolerable. The 13-level inverter structure performed well in simulations with various loads. The proposed SC-MLI is shown to be superior to other inverter topologies in studies evaluating their ability to reduce the inverter system's footprint, bill of materials, number of power switches, and voltage stress on the switches. [3]

M. Venkatesan et. All (2022) This study suggests a SC inverter design that, without the need for a large transformer, can generate outputs of different magnitudes from a relatively low input voltage (50 V). Multicarrier pulse width modulation was used to regulate the SC inverter. Since the stress voltage of the switches is not more than the applied voltage in the absence of H-bridges, the total standing voltage of the inverter is also much reduced. The proposed inverter requires just 50 V of DC input to generate a single-phase, 50 Hz, AC output voltage. The traditional inverter is now smaller and lighter in weight. That's why the proposed SC inverter is compatible with so many different SAPFs. To check the accuracy of the simulations, we used MATLAB/Simulink. [4]

Ravi Anand et. All (2022) This paper proposes a different topology for SCMLI. The described circuit is able to create nine different output voltages from a single direct current (DC) input by multiplying it by four. In this case, an H-bridge is not required because both positive and negative cycles may be generated without one. Because the capacitors in this design operate in parallel, automated balancing and reduced TSV are both possible. The number of switches is a key component of this design. This article also covers the expanded version of the suggested architecture, which adds switches and capacitors to try to maximise the possible gain. The suggested topology has been extensively compared to the current recommended SCMLI topology. The findings of this study provide strong evidence in favour of adopting the recommended topology. The pulse logic decoder generates PWM signals by comparing a number of carrier signals to a standard sinusoidal reference signal. This method is best described as a pulse-width modulation with a level shift. The prototype created in the lab is tested in the field to see how well it performs. [5]

Suresh Velliangiri et. All (2021) The effectiveness of the proposed 9L-SCMLI design has been evaluated by modelling and simulation testing in the MATLAB/SIMULINK software package. Through computational modelling, we know that the planned converter produces a multilayer voltage output with low harmonic distortions. Medium-power, high-voltage applications benefit greatly from this design. The output voltages from several trials using different switching sequences have been recorded and graphed. Various converters have been compared to the proposed converter. The 9L-SCMLI converter is recommended since it is better than the other MLI formats, according to the research. [6]

Junfeng Liu et. All (2014) In this work, we present a new SC-based multilayer cascaded inverter. The 9-level and 13-level circuit topologies are analysed thoroughly. The number of switching devices in the

proposed inverter may be drastically reduced in comparison to a traditional cascaded multilevel inverter. The low switching frequency and straightforward design of a single carrier modulation scheme called symmetrical PSM were proposed. Consistent modelling and experimental findings support the practicality of the suggested circuit and modulation approach. SC frontend allows for a greater range of voltages than a standard cascade H-bridge. For example, in a 9-level circuit, the number of voltage levels doubles every half cycle, while in a 13-level circuit, it triples every half cycle. [7]

Mohammad Fahad et. All (2022) We have examined a multilayer multisource step-up inverter that has few components yet produces high-quality electricity. We show that the suggested SCMLI works, and that the capacitor voltages can balance themselves out. The benefits and drawbacks of previously developed MLIs and switched-capacitor setups are explored. Recent topologies were compared to the proposed SCMLI. To demonstrate the topology's thermal behaviour and efficiency, a thermal loss study was performed. The outcomes of our simulations are shown here. The performance at varying loads and MI has been verified experimentally. [8]

Yaoqiang Wang et. All (2020) In this work, we introduce a generalised T-type switched capacitor module (TSCM) multilevel inverter. The suggested inverter's operating principle and modulation approach were examined using a nine-level inverter as a case study. Since the voltage divider capacitors' positive and negative halves act in a symmetrical fashion, the voltage may balance itself. By charging the switching capacitors in stages and designing the proposed inverter to be easily expanded, it is possible to boost both the output voltage and the voltage gain. The suggested inverter can minimise the number of devices, which in turn reduces the capital cost and power losses, as shown by comparisons with other current topologies. In addition, when the output voltage rises, the suggested inverter's number of switches and capacitors increases along a logarithmic curve. In other words, when the output voltage is high, the author's technique is more common than alternative topologies in terms of the devices utilised. The inverter may be conveniently miniaturised with the help of the modular expansion approach. [9]

Safwan Mustafa et. All (2023) This article presents a new method for building boost inverters, using a quadruple-boost voltage waveform with nine stages. Conventional MLI suffers most when switching to renewable energy sources due to the requirement of a high voltage DC-DC converter to boost the voltage. Thus, the discovered technology, with its capacity to automatically enhance the input voltage by a factor of four, may make up for that deficiency. The revised design only requires one DC power supply, two switching capacitors, and eleven switches. The capacitor's voltage finds its own equilibrium on its own. The DC source in a conventional MLI is replaced with a capacitor in a switched capacitor MLI, which reduces the number of components needed. The nine-step output voltage waveform requires precise charging and discharging of the switching capacitor. The SPSC mechanism allows for such progress to be made. Parallel and series coupling of switched capacitors in the conduction channel increases the voltage. Different factors based on the number of components, total harmonic distortion (THD), and cost have been used to evaluate the quality of this suggested topology, and the results show an efficiency of 97.85%. The suggested method's switching order is regulated using the Nearest Level Modulation Technique (NLC). The Nine-level converter was tested with the help of MATLAB and PLECS. [10]

Prabhat Ranjan Bana et. All (2020) With only two dc sources and a handful of switches, this study presents a new DSC MLI capable of outputting a 25-level staircase. The number of sources may be greatly reduced by using capacitors to synthesise the voltage levels. By strategically placing the SCs, we may increase the voltage with no need for extra voltage balancing circuits. The suggested DSC MLI therefore achieves the best possible balance between size and cost. We have analysed three potential additions to the suggested architecture to increase the voltage levels. By evaluating the suggested topology against the standard MLI topologies, we confirm that it makes use of fewer components and places less strain on the switches. In addition, the suggested MLI has lower conduction loss since fewer than half of the switches are in conduction when synthesising any voltage level. [11]

Hassan Yousif Ahmed et. All (2022) This study introduces a multilayer inverter with two stages of

boost. The first stage uses a SC-Boost converter to increase the PV panel's low voltage and maximise power extraction, and the switched capacitor from that stage is used as an input for the second. A new seven-level multilevel inverter is used to build the second stage of the two-stage inverter, which in turn generates a voltage spectrum with seven discrete levels. Unique characteristics of the suggested seven-level inverter are its small size, low cost, decreased number of switches, and lower condition loss. This is so because its eight potential switching states are implemented with only seven switches. Three switches are always active in each switching mode. The switches of the multilayer inverter are driven by a pulse width modulator (PWM) that uses a level shift. [12]

Manjunatha Budagavi Matam et. All (2018) In order to improve upon traditional and newly reported multilevel inverters' lacklustre boost capabilities, this research offers an Impedance Source Switched Capacitor Multilevel Inverter. Using just a single input and a single impedance network, seven distinct output levels may be generated. Using a self-voltage balance circuit, we can produce a voltage that is balanced across all of the capacitors. We charge all the capacitors to 50% of their input voltage. In contrast to standard MLI, only (n-1) of the switches are conducting at any given time. As a result of all the switches being run at a lower frequency, switching losses are reduced. After developing the experimental setup using simulation settings, it is discovered that the two sets of results are very congruent. [13]

F. Sedaghati et. All (2022) In this study, a unique multilevel inverter utilising a switched-capacitor architecture that is also capable of boosting is presented. Using just a single DC voltage source as input and a boost factor of 3, the proposed converter can generate seven distinct levels of output voltage. Switch pulses are generated via closest level modulation. Extended symmetric and asymmetric topologies of the described SC multilevel inverter are shown to generate voltage waveforms with 17 and 31 levels, respectively. To highlight the benefits of the new multilayer inverter, a comparison is made to similar architectures. The proposed inverter was eventually built on a smaller scale in a lab and put through a battery of tests to verify its efficacy. [14]

Shivaprakash. T et. All (2021) Therefore, the suggested inverter can generate the seven-stage output voltage using fewer parts. The inverter uses either a symmetric or an asymmetric DC input to power an alternating current load. When compared to other topologies, this one reduces THD by 21.44 percent, and its seven-stage output means it can be used for applications requiring low, medium, or high power output. It is also very cost-effective, as it eliminates the need for a large number of power switches and reduces the number of protection circuits. The suggested design uses only two capacitors, whereas a typical capacitor-clamped multi-level inverter would require many more. C1 and C2 are able to handle the whole positive and negative cycle. [15]

3. Multilevel Inverter Topologies

Conventional inverters are briefly described in this chapter along with their benefits and drawbacks. Different multilevel inverter topologies and their underlying principles are covered in this article. The primary limitation of multilayer inverters is the escalating switch count as more levels are added. Control circuitry creation for a high number of power switches was a major challenge in the early days of multilevel inverters. However, this problem has been quickly resolved because to the rapid development of CPLD, DSP, and FPGA devices. Another limitation of this inverter is that it needs several DC voltage sources, primarily capacitors. One of the most difficult aspects of operating is maintaining voltage source balance under varying loads. Even with these constraints, however, power device switching losses can be reduced by using multiple inverters. The filter size needed to get rid of harmonics is less than what's needed for two-level inverters. The size, cost, and weight of the inverter are all reduced as a result. There have been several proposals for multilayer inverter topologies during the past two decades. New modulation techniques and inverter topologies have emerged as a result of recent scientific inquiry. In addition, three distinct primary multilevel inverter architectures have been identified. They are

- "Diode clamped /Neutral clamped Multilevel Inverter"
- "Flying capacitors /Capacitor clamped Multilevel inverter"
- "CascadedH-bridge Multilevel Inverter"

3.1 Multilevel Concept

For high output, a multilayer inverter often uses a staircase voltage waveform synthesised by a series of power semiconductor switches connected to many low voltage DC sources. Figure2 depicts a multilayer inverter's phase one leg. An ideal switch with several states represents the actions of semiconductors in this figure.

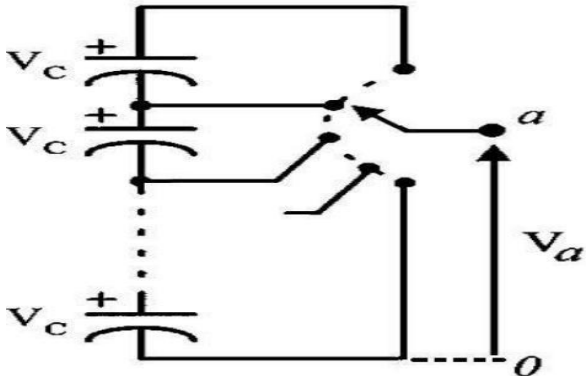


Figure: 2 One phase leg of a multilevel inverter

Multilevel inverters have been employed in the field of power electronics for close to three decades. Their names reflect the number of output voltage levels and the various topologies they employ. The number of available voltage levels at the output is typically not even but odd. This implies that the output of the inverter is more sinusoidal and has fewer harmonics when a zero voltage level is defined, as is the case with three-level and five-level inverters.

3.2 Diode Clamped Multilevel Inverter

Neutral-point converters, a topology pioneered by Nabae, Takahashi, and Akagi in 1981, are widely used in a wide variety of power and industrial applications.The diode-clamped multilevel inverter utilises clamping diodes and cascaded dc capacitors to create ac voltage waveforms with many levels. However, as the number of levels increases, the circuit layout gets more complicated, requiring more clamping diodes, switching devices, and dc capacitors. For every m legs of an m-level diode clamped inverter, there must be m-1 clamping diodes and m-1 dclink capacitors. Due to the unequal load distribution among the semiconductor switches, reverse recovery of the clamping diodes is also a crucial design difficulty when the inverter runs utilising the pulse width modulation (PWM) technique. Even though the NPC architecture is easy to use, more equipment is required as the number of inverters increases. The planning and execution get more difficult as the number of levels grows.

3.3 Flying Capacitor Multilevel Inverter

The Flying capacitor, also known as the capacitor clamped inverter architecture, was suggested by Meynard and Foch in 1992.This inverter design is quite similar to the NPC topology, with the exception of the clamping diodes. In this inverter topology design, capacitors are used in place of clamping diodes. Different voltages are applied across each capacitor in a ladder configuration on the dc side of a flying capacitor MLI. The flying-capacitor design features phase redundancies for internal voltage levels, unlike the diode-clamped inverter's sole line-line redundancies. So, two or more possible switch configurations exist for synthesising an output voltage.For an m-level output phase voltage, you'll need (m-1) * (m-2)/2 auxiliary capacitors per phase on top of the (m-1) maindc link capacitors, assuming the capacitors have the same voltage ratings as the main switches.

3.4 Cascaded H-Bridge Multilevel Inverter

An advanced piece of power electronics, a Cascaded H-Bridge Multilevel Inverter can transform DC current into AC current with increased voltage and less harmonic distortion. Multiple H-bridge modules are linked in series to produce this novel inverter architecture; these modules individually contribute to the whole output voltage waveform. Stepped multilevel AC waveforms with more voltage steps than conventional inverters may be synthesised by manipulating the switching states of these H-bridge cells. In addition to allowing for larger voltage outputs to be generated, this method also improves voltage quality, decreases harmonic distortion, and boosts efficiency. Since they can generate high-quality AC waveforms, Cascaded H-Bridge Multilevel Inverters are a compelling option for achieving reliable and optimised energy conversion in a variety of contexts, such as renewable energy systems, high-power motor drives, and grid-connected systems.

4. E-TYPE MLI

This work presents a novel topology of asymmetric multilevel modular with a new component arrangement, dubbed Envelope type(E-Type), that consists of 10 switches, 10 diodes, and 4 unequal DC sources (22,21V). This set-up, which synthesises voltage sources, generates 13 levels (including zero)

without the use of an extra circuit. The primary idea behind this circuit is to link sources from opposite sides of a DC power supply. The E-Type asymmetrical module's layout is seen in Fig. 3; the centre DC sources are grouped with other switches (S1-S6) to provide a range of voltages. A two-way switch (S7) is needed to prevent the DC sources on the left and right sides of the module from shorting out. To go to 5 voltage, you'll need another bidirectional switch (S8).

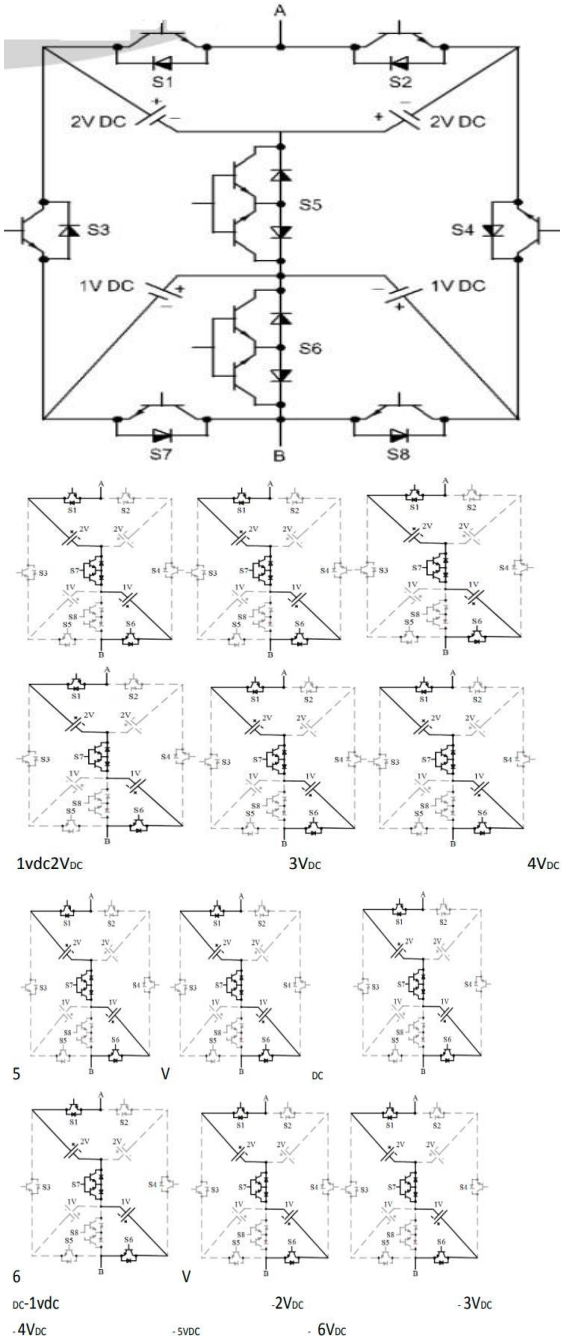


Figure: 3 Existing E-Type module inverter circuit topology and different switch status

		"S1"	"S2"	"S3"	"S4"	"S5"	"S6"	"S7"	"S8"
POSITIVE LEVEL"	**"1VDC"**	1	0	0	0	0	1	1	0
	"2VDC"	1	0	0	0	0	0	1	1
	"3VDC"	1	0	0	0	1	0	1	0
	"4VDC"	1	0	0	1	0	1	0	0
	"5VDC"	1	0	0	1	0	0	0	1
	"6VDC"	1	0	0	1	1	0	0	0
EGATIV ELEVEL"	**"-1VDC"**	0	1	0	0	1	0	1	0
	"-2VDC"	0	1	0	0	0	0	1	1
	"-3VDC"	0	1	0	0	0	1	1	0
	"-4VDC"	0	1	1	0	1	0	0	0
	"-5VDC"	0	1	1	0	0	0	0	1
	"-6VDC"	0	1	1	0	0	1	0	0

Table I Switching Table

Table I shows the corresponding levels for the S1 and S4 switches. Also, you can't have both (S1, S2) and (S3, S4) active at the same time.The pulse pattern associated with the proposed inverter's output voltage is seen in Fig.4 for one cycle of the fundamental voltage. Switches S1, S2, S3, S4, and S7 are repeatedly switched on and off at low frequencies to minimise switching losses, as seen in Fig. 4. The switching frequency of other switches is likewise generally acceptable. Table II details the number of voltage levels, semiconductor components, DC sources, and drivers required for a given configuration, where n and NL are the desired and required numbers of module units.

	"BASED ON NUMBER OF MODULE UNITS"	"BASED ON NUMBER OF DESIRED LEVELS"
"Levels"	13n+1	N_L

"Number of Switches"	10n	$5(N_L -1)/6$
"Number of Diodes"	10n	$5(N_L-1)/6$
"Driver"	8n	$8(N_L-1)/6$
"Number of DC Links"	4n	$4(N_L-1)/6$
"TSV"	20n	$10(N_L-1)/6$

Table II Equation of e-type module

5. Terminology, Assessment Parameters And Classification Of Topologies

Some words related to the evaluation criteria are established before a comparative study of topologies is conducted. After that, we talk about the many criteria that may be used to evaluate lower device count topologies, and then we classify the topologies so that a general picture can be painted.

A. Terminology

(a) Reduced Device Count Multilevel Inverter (RDC-MLI) Topologies: By "RDC-MLI topologies," we mean those that suggest or offer a reduced number of controlled switching power semiconductor devices for a fixed number of phase voltage levels.

(b) Total Voltage Blocking Capability: The "total voltage blocking capability" of a topology is the sum of the voltage blocking capabilities of all its power switches. To illustrate, let's say a building needs a voltage blocking capability of [(4 X VDC) + (6 X 2VDC) = 16VDC] since it has four switches rated at VDC and six switches rated at 2VDC.

(c) Symmetric and Asymmetric Source Configuration: An MLI has a symmetric source configuration if and only if the DC voltages at each input are identical. Binaries and ternaries are two common types of asymmetrical source arrangements. The voltage levels in a binary arrangement increase by a factor of two (i.e., VDC, 2VDC, 4VDC, 8VDC...), but in a trinary setup the GP factor increases by a factor of three (i.e., VDC, 3VDC, 9VDC, 27VDC...). Different academics have proposed a wide variety of different arrangements for asymmetric sources. Using an asymmetric source design, we can generate additional output levels while keeping the number of power switches same.

(d) Even Power Distribution: It is claimed that the "power distribution" among the sources is "even" when the multilevel DC-to-AC conversion is performed in such a way that each input source gives the same amount of power to the load. The term "charge balance control" or "equal load sharing" is also used by certain writers to describe this concept. Control aspect includes "even power distribution," but only if the architecture allows it. When there is symmetry between the source configuration and the control method, the average power consumed from each source will be the same. If each input source contributes to all output levels in one or more output cycles, then the power may be distributed evenly for that structure. For instance, if the topology allows for all the options listed in Table I, then the power may be distributed evenly if the input DC sources are symmetric (VDC,1 = VDC,2 = VDC,3 = VDC).

"Output voltage level"	"Required combination of input DC levels"
"±*VDC*"	"± *VDC,1*"
"±*VDC*"	"± *VDC,2*"
"±*VDC*"	"± *VDC,3*"
"±2*VDC*"	"± (*VDC,1* + *VDC,2*)"
"±2*VDC*"	"±(*VDC,2* + *VDC,3*)"
"±2*VDC*"	"±(*VDC,1* + *VDC,3*)"
"±3*VDC*"	"±(*VDC,1* + *VDC,2* + *VDC,3*)"

Table: 3 Example Of Possibility Of „Even Power Distribution"

When Three Input Sources Vdc,1 = Vdc,2 = Vdc,2 = Vdc Are Available

(e)Level-Generation and Polarity-Generation: An MLI creates a stepped waveform using the sums and/or differences of the input DC levels. The voltage waveform, then, consists of a number of "levels," some of which are positively charged while others are negatively charged (during the opposite halves of the cycle). An H-bridge is often used to convert the unipolar waveform produced by the MLI circuit into a bipolar waveform suitable for driving an alternating current (AC) load. The "level-generation part" and the "polarity-generation part" are the names given to these components. The power switches used in the polarity generating section must be able to handle at least the same voltage as the MLI itself.

(f) Fundamental Frequency Switching: The switching losses of a converter are based on its current, blocking voltage, and switching frequency. Power

switches with a higher voltage rating can decrease switching losses by operating at a low frequency, ideally the power frequency (or fundamental frequency), without negatively impacting the quality of the output waveform. A power switch in a topology can work at fundamental switching frequency if it remains ON for a whole half cycle (positive or negative) and then OFF for the following complete half cycle; this allows the load terminals to synthesise the proper multilayer waveform. In other words, the modulation scheme can have some degree of control over the fundamental frequency switching frequency if the architecture permits it. Furthermore, in a topology with power switches of varying voltage ratings, the switching losses should be distributed uniformly by operating the switches with higher voltage ratings at lower switching frequencies and the switches with lower voltage ratings at higher switching frequencies. This means the switching frequency should be "distributed" according to some established method if the network structure allows for it. If a topology's level generator can also synthesise the zero level, then polarity generator switches can be operated at line frequency.

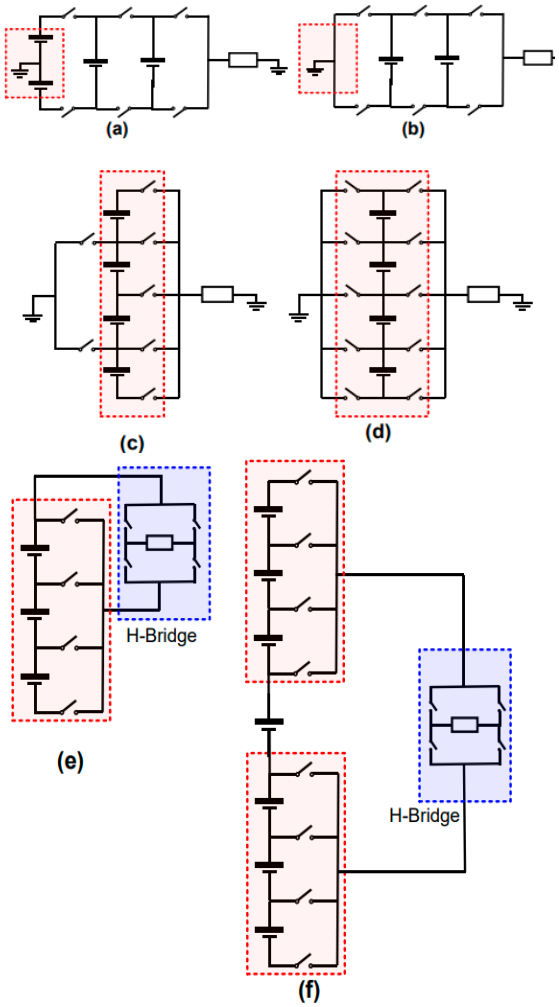
Assessment Parameters

The primary criterion for evaluating the quality of a topology is the task for which it was designed. However, for the purposes of this article, the following criteria may be used to make a broad comparison of the RDC-MLI to the other topologies and determine whether or not it is superior:

i. “The number of power switches used”.
ii. “The total blocking voltage of the converter”.
iii. The topology's optimal controllability in terms of charge-balance control (or "even power distribution" among the input sources) and the proper distribution of switching frequencies among the differentially voltage-rated switches.
iv. “Possibility of employing asymmetric sources/capacitorvoltage ratios in the topology”.

Parameter (iii) governs the application, performance, and control complexity of the inverter, whereas parameters (i) and (ii) determine the inverter's dependability. Both (i) and (iv) have a significant impact on the total number of redundant states and, by extension, the tunable nature of fault-tolerant operation. In addition to (i) and (ii), the cost of a converter also depends on the variation in power switching ratings (e.g., it would be more costly to use one 400V switch and one 800V switch than it would be to use two 600V switches).

The similarities between the different RDC-MLI topologies become clear when they are drawn consistently, ignoring the peculiarities of the power switch arrangements. As shown in Fig.4(a) and (b), for instance, the PUC design is equivalent to the flying capacitor layout when no DC power sources are present. As can be seen in Fig. 4(c) and (d), T-type inverters and CBSC-based MLIs share similar modules. The 2SELG based MLI is built by repeatedly connecting the same units as the MLM based MLI, as shown in Fig. 4(e) and (f). The topologies provided in are shown in Fig.4 (g), (h), (i), and (j) by analogous but differently connected arrays of sources and switches. The RDC-MLI topologies can be classified as either H-bridge-based or non-H-bridge-based (see Fig.4). It's also feasible that these architectures need DC input levels that aren't isolated. This comprehensive grouping of RDC-MLI topologies is depicted in Figure 5.



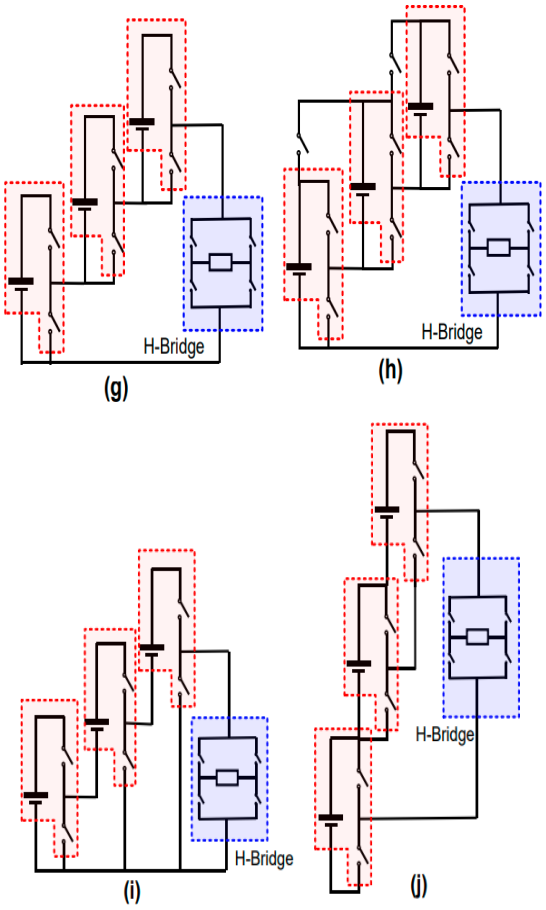


Figure: 4 Similarities in the structures of various topologies

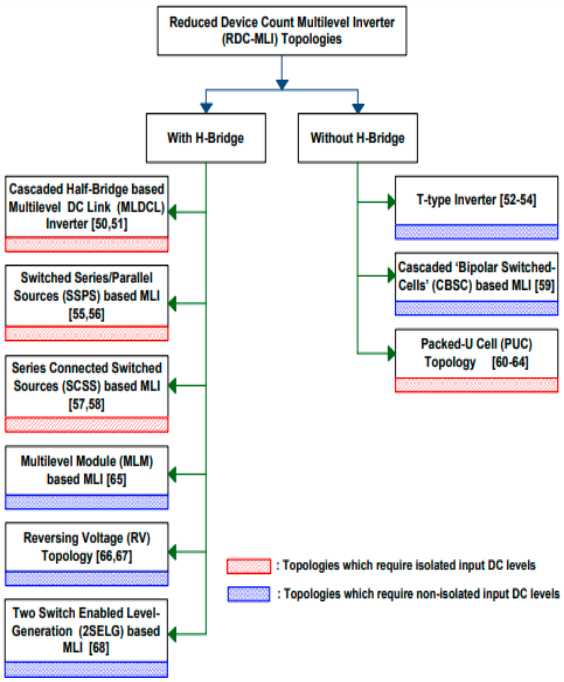


Figure: 5 Categorization of reduced device count multilevel inverter (RDC-MLI) topologies

Conclusion

A considerable number of SC-MLIs have been introduced after more than a decade of fast development. Due to the large number of SC-MLI topologies and the lack of a systematic evaluation, this paper provides the first attempt at defining the current state and future research directions for this emerging family of MLIs. Almost all of the existing topologies are thoroughly categorised, and the idea of incorporating SC-based basic units into various circuit configurations of MLIs is addressed critically. In this study, we take a quick look back at the state of the art in SC-multilevel inverter research. The primary goal of this analysis is to acquire useful knowledge about recent topologies for the purpose of making an informed decision when selecting an MLI topology. By contrasting these topologies with traditional MLI topologies, the benefits of switched-capacitor-based MLIs become clear. Numerous academics have presented topological methods for multilevel inverters that are optimised for either high or low power consumption. In addition, recent proposals have made use of multilayer topologies to provide excellent output resolution with fewer power switches.

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