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Implementation of 16 Bit SFRG Test Patterns for Detecting Faults on LBIST

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Abstract: Defects have increased as a result of manufacturing issues brought on by the ever-increasing transistor count on chips and the shrinking feature size. For any Very Large Scale Integrated (VLSI) design, testing has thus become essential. Due to the length of the design cycle, the test procedures used to test those designs are disregarded as the design engineers focus more on design development. Any design must be 100% fault-free in order to pass, and the Design for Testability (DFT) technique makes it easier to find the errors. Different standards have been developed to test various integrated circuit components. In this paper fault coverage of Logic Built In Self-Test (LBIST) is designed and implemented for 16 bit test pattern using SFRG to get maximum fault coverage with detection of faults compare to other Pattern generators and it also gives the area, power and better efficient using this test pattern. The design is coded in Verilog, verified for functionality using Xilinx ISIM simulator.

Index Terms : Seed Flipping in Ring Generator, Built-in Self Test (BIST), and Logic Built-in Self Test are some index terms (LBIST).

Introduction

In the design of high performance very large scale integration (VLSI), low power design has grown urgent and difficult in recent years. As a result, numerous methods have been devised to reduce the power consumption of new VLSI designs. While test mode operation hasn't been a big focus of research, most of these ways are suggested to cut power usage during functional operation. Recent research reveals that switching activity is frequently substantially higher during test mode operation than it is during functional operation. An increase in peak power dissipation could result in an inductance-related voltage decrease. This could then result in some good die failing the test, causing an unwarranted loss of yield. A circuit under test (CUT) may become less reliable and potentially sustain damage as a result of increased average power dissipation, temperature, and current density. Testing VLSI devices at a high level costs more money as their size and complexity increase.Nevertheless, it is uncertain whether test compression will be able to keep up with the tremendous pace of technological advancement during the ensuing ten years. It's interesting to note that logic built-in self-test (LBIST), which was first created for board, system, and in-field testing, is now being accepted for production testing because it offers extremely reliable DFT and is utilized more frequently with test compression. This hybrid strategy appears to be the logical advancement of DFT. It has the potential to increase test quality, increase the speed at which power-aware tests may be done, and lower the cost of manufacturing testing while maintaining all LBIST and scan compression benefits.VLSI circuit complexity is constantly rising, necessitating the adoption of a built-in self-test (BIST). The chip can test itself and assess how the circuit reacts thanks to built-in self-test. Many different BIST equipment design methodologies have been offered. Most cutting-edge techniques use some sort of pseudorandom pattern generator (PRPG) to create test vectors for the circuit. These vectors are applied to the circuit either as they are, or the vectors are modified by some additional circuitry in order to obtain better functional coverage.

Project's Objective And Scope

This paper's primary goal is to produce test patterns of 16-bit Seed to detect the fault with maximum fault coverage of any VLSI Circuit with low power and efficient .

Seed Flipping Test Pattern Generation

This polynomial equation was created by 16-bit SED utilizing $X^{16}+X^{15}+X^{13}+X^{4}+1$, and we may generate random outputs for it. You may view the 16-bit SEED circuit diagram in Power reduction is mostly influenced by the unique technological characteristics of the used gates. The SEED uses an XOR gate as part of its input. Its output is a flip-flop with a pre-loaded seed value that can be any number other than zero.The ones in the

polynomial match the input of the initial bit. Polynomial term powers are expressed using tapped bits starting from the left. The input and output taps are always connected to the first and last bits, respectively. There must be an even number of taps and a common divisor among all taps for the length to be at its maximum. A 16-bit SEED that produces 216 -1=65535 random outputs has a maximum feedback polynomial length of $X^{16}+X^{15}+X^{13}+X^{4}+1$. Figure depicts a 16-bit SEED circuit with maximum length feedback, which causes the SEED to only produce 0 patterns. When the SEED is timed, the PRPG produces 0s and 1s. using the 16-bit seed of the fundamental polynomial $X^{16}+X^{15}+X^{13}+X^{4}+1$.

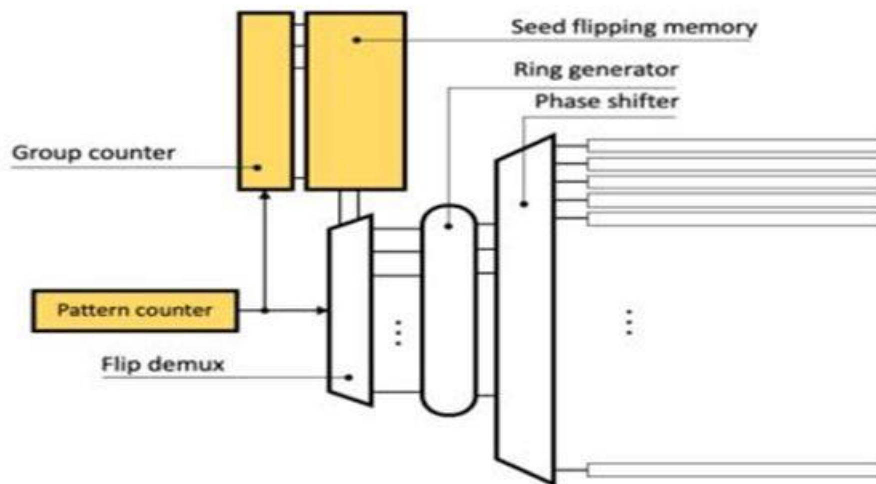

Fig1. SEED Flipping Architecture

In this case, eight more XOR gates are added so that each flip-flop inverts its output and transmits it to its neighbor to the right. A stage of the ring generator is then inverted if one of the flip-output demultiplexers asserts. The little difference in implementation must be kept in mind at all times. An investigation to confirm every VLSI testing issue was carried out in order to discover dependable testing techniques that would lower the cost of test equipment.

LBIST

The need of outdoor testing is occasionally neglected in favor of test data size and fitting into testers' capabilities. There is a developing market for automobile design where the necessity of field testing the digital logic is being stressed more. Logic that is controlled by digital signals is taking the place of tried-and-true mechanical devices. Automotive manufacturers are pursuing this route in an effort to improve user experiences, lighter designs, and fuel efficiency. Throughout the life of the car, these systems must be highly reliable. A vital digital system's ability to function as intended can be compromised by flaws brought on by heat, exposure to the environment, and time. For vehicle manufacturers, finding these flaws before a serious failure is of the utmost importance. Together with Cadence's Encounter Test's DFT and ATPG system, a large automotive chip manufacturer was able to integrate an effective direct access LBIST into its car design, which demands great dependability throughout the product's lifespan. The digital logic can be tested using the LBIST, which also generates a go/no-go signal to show whether the logic is still operating as it was designed to.

Implementation Of Seed Flipping For Detecting Faults On LBIST

The LBIST architecture under consideration is seen in Figure. 1. Test Pattern Generator (TPG): In testing mode, TPG assists in generating input patterns for LBIST. The TPG under consideration is a 16-bit SEED that generates all (2n) states in a pseudo-random way. A compression method

called Output Analyser is utilized to extract a signature from the DUT's outputs. Depending on whether the LBIST is being used in normal mode or testing mode, the TEST controller is set up to activate the appropriate blocks. In order to choose between the Pattern inputs and the System Inputs , a multiplexer (MUX) called a 2X1 MUX is needed. Since the SEED is 16 bits in size, the input to the MUX is 16 bits in size. As a vector is used as the input data for MUX, a vector is also used as the output data. Test Controller is in charge of controlling the MUX's choose signal. The 16 bit multiplier is the design that will be tested since, according to research, it is one of the quickest multiplies. This is because multipliers are frequently used in DSP applications. Since the multiplier is 16X1, it needs two inputs that are each 8 bits in size. The higher nibble is supplied as one input and the lower nibble is provided as another input because the output of the MUX is 16 bits. The comparator receives a straight 16-bit feed from the multiplier. Comparator is used to generate the status of testing of fault and fault free circuits .If f1 is 1 then the fault is present if f2 is 0 then the
Circuit is fault free

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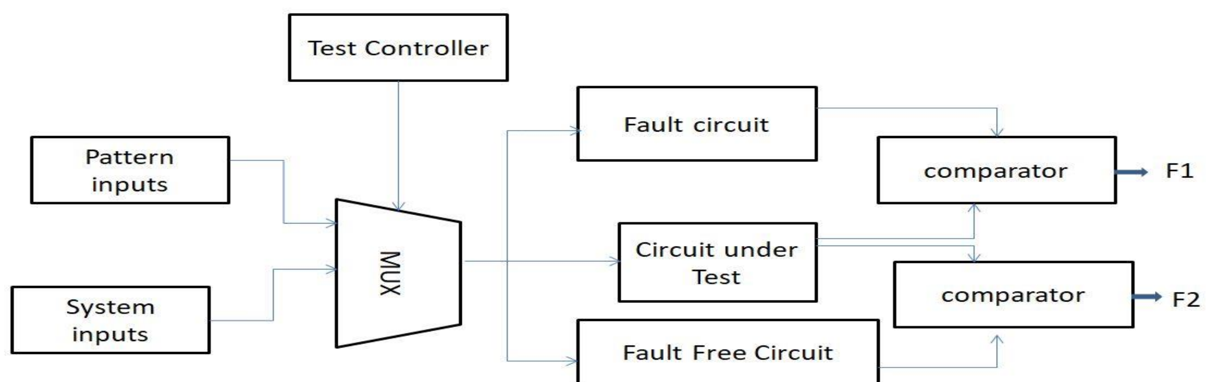

Fig2. LBIST Architecture For Detecting Fault

Simulation Results

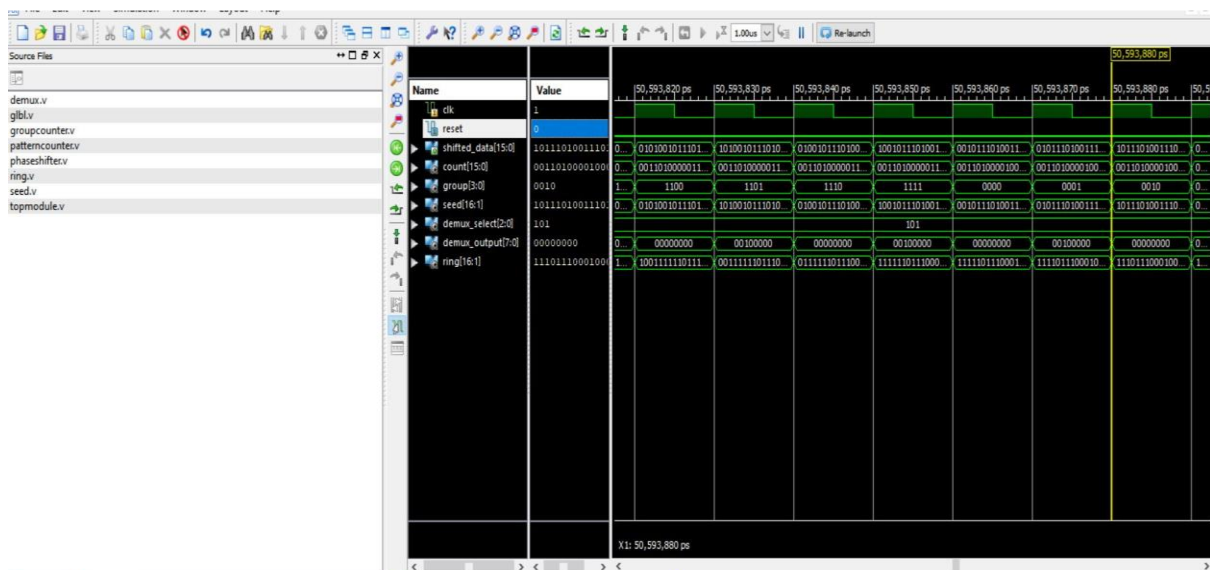

Fig3. Represents Simulation for Test Pattern Generation of Seed Flipping

Fig4. Represents Simulation For Fault free Circuit

Fig5. Represents Simulation Result of Fault Circuit and fault free ciruicit

Conclusion

The designs are getting more complicated to satisfy customers' more demanding expectations. The complexity of chip design makes the production process challenging and could result in subpar semiconductors. The current trend is toward fault-free design to increase chip yield. Create for In order to optimize the yield process, test techniques that are necessary to find faults and in certain circumstances, rectify them are also integrated. Since it affects test cost and quality, power consumption during testing mode must also be taken into account. For 16 bit test pattern using SFRG, (LBIST) is created and implemented to provide maximal fault coverage with fault detection.

References

[1] Design and Analysis of Test Pattern Generator by Combining Internal and External LFSR, Chinnapapakkagari Sreenivasa Vikranth, 2021. Ring generators—New devices for embedded test applications, IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 23, no. 9, pp. 1306–1320, September 2004.

[2] Ms. G. Suneetha, Dr. B. Leela Kumari, Mrs. T. V. Ramani, IMPLEMENTATION OF 16 BIT SFRG TEST PATTERNS FOR DETECTING FAULTS Industrial Engineering Journal ISSN: 0970-2555 Volume : 52, Issue 8, No. 4, August : 2023

[3] G. Mrugalski, J. Rajski, and J. Tyszer, ―Ring generators—New devicesfoembedded test applications,‖ IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 23, no. 9, pp. 1306–1320, Sep. 2004

[4] Paritala Avinash Kumar, J. P Anita Department of Electronics and Communication Engineering,Amrita School of Engineering, Coimbatore,Amrita Vishwa Vidyapeetham, India .‖Implementation of Hybrid LBIST Mechanism inDigital Circuits for Test Pattern Generation and Test Time Reduction ―mainly used to test the circuits. Proceedings of the Fifth International Conference on Communication and Electronics Systems (ICCES 2020)IEEE Conference Record

[5] Adithya Kashyap R, S. GayathriJSS science and technology JSS science and technology Mysuru, India Mysuru, India.‖Study on LBIST and comparisons with ATPG

[6] Abhilash Bagalkoti Dept. of ECE, Suhas B Shirol Dept. of ECE, BVBCET Ramakrishna Dept. of ECE Rajashekar B S Dept. of ECE, Priyatamkumar Dept. of ECE, ―Design and Implementation of 8-bit LFSR, Bit Swapping LFSR and Weighted Random Test Pattern Generator: Performance Improvement‖International Conference on Intelligent Sustainable Systems (ICISS 2019)IEEE Xplore

[7] P.Wohl, J.A. Waicukauski, G.A. MastonSynopsys, Inc.J.E. ColburnNVIDIA Corp.‖XLBIST: X-Tolerant Logic BIST‖Paper 13.1 INTERNATIONAL TEST CONFERENCE ©2018 IEEE

[8] Design and Implementation of Power Efficient Logic BIST With High Fault Coverage Using Verilog conference paper 2018

[9] Test pattern generation using thermometer code counter in TPC technique for BIST implementation K. Jamal a (elsevier.com)2019

[10] R. Dorsch and H.-J. Wunderlich, "Tailoring ATPG for embedded testing," in Proc. IEEE Int. Test Conf. (ITC), Baltimore, MD, USA, 2001, pp. 530–537.

[11] D. Xiang, X. Wen, and L.-T. Wang, "Low-power scan-based built-in self-test based on weighted pseudorandom test pattern generation and reseeding," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 3, pp. 942–953, Mar. 2017

[12] M. Chatterjee and D. K. Pradham, "A novel pattern generator for near perfect fault-coverage," in *Proc. 13th IEEE Very Large Scale Integr. (VTSI) Test Symp.*, Apr./May 1995, pp. 417–425.

[13] D. Das and N. A. Touba, "Reducing test data volume using external/ LBIST hybrid test patterns," in *Proc. Int. Test Conf. (ITC)*, 2000, pp. 115–122.

[14] R. Dorsch and H. Wunderlich, "Tailoring ATPG for embedded testing," in *Proc. Int. Test Conf. (ITC)*, 2001, pp. 530–537.

[15] P. Girard, L. Guiller, C. Landrault, and S. Pravossoudovitch, "A test vector inhibiting technique for low energy BIST design," in *Proc. 17th IEEE VLSI Test Symp. (VTS)*, Apr. 1999, pp. 407–412.

[16] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H.-J. Wunderlich, "A modified clock scheme for a low power BIST test pattern generator," in *Proc. 19th IEEE VLSI Test Symp. (VTS)*, May 2001, pp. 306–311

[17] S. Hellebrand, H.-G. Liang, and H. Wunderlich, "A mixed mode BIST scheme based on reseeding of folding counters," in *Proc. Int. Test Conf. (ITC)*, 2000, pp. 778–784.

[18] S. Hellebrand, J. Rajski, S. Tarnick, S. Venkataraman, and B. Courtois, "Built-in test for circuits with scan based on reseeding of multiple polynomial linear feedback shift registers," *IEEE Trans. Comput.*, vol. 44, no. 2, pp. 223–233, Feb. 1995.

[19] B. Koenemann, "LFSR-coded test patterns for scan designs," in *Proc.Eur. Test Conf. (ETC)*, 1991, pp. 237–242.