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Digital Circuits Layout Design using Transistor Sizing

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Abstract

This paper introduces a novel heuristic transistor sizing technique aimed at optimizing Very LargeScale Integration (VLSI) circuit designs within the framework of a standard cell design approach. Inherent in this approach is the challenge of managing transistor dimensions to mitigate unnecessary upsizing and downsizing, which can lead to unwarranted increases in transistor widths. The proposed technique not only effectively addresses this challenge but also yields significant improvements in circuit delay and power efficiency. To validate the proposed method, the study focuses on the layout design aspect, utilizing the cadence virtuoso-90nm platform and leveraging the Ncell and Pcell methodology. This strategic approach results in an impressive 34% reduction in overall layout area, showcasing the practical utility of the heuristic transistor sizing technique. Additionally, by implementing the transistor sizing strategy judiciously, the paper attains notable reductions of 4-15% in both circuit delay and power consumption. The findings of this research underscore the substantial impact of the proposed approach on VLSI circuit optimization. By offering a solution to the transistor sizing challenge and its subsequent effects on circuit performance, this work provides a valuable contribution to the field, presenting a comprehensive method for enhancing the efficiency and effectiveness of VLSI circuit design.

Keywords—Heuristic, Cadence, VLSI, NP Methodology, DRC(Design Rule Check), LVS(Layout Versus Schematic).

Introduction

Standard cell-based design methodologies are widely adopted and effective in streamlining the Very-Large-Scale Integration (VLSI) layout design process. They enable efficient power and ground pin connections within standard cell instances by organizing instances into rows. These rows are then integrated with horizontal power and ground lines, simplifying the intricate task of designing the overarching Power/Ground rings that encompass the layout [2][9]. Successful standard cell placement strategies optimize the arrangement of individual transistors, offering the potential for deliberate modifications that minimize overall layout area [3][4][5].

To meet stringent timing requirements and curtail system power consumption, the flexible adjustment of transistor sizes within instances is pivotal. This involves both upscaling and downscaling transistors. Substituting sets of instances with meticulously optimized alternatives can further curtail delay and power dissipation [6][7][8].

However, precise transistor sizing remains a challenge due to the pervasive role of standard cells in VLSI design, shaping all facets of the design and optimization process. For instance, achieving optimal sizing for an inverter necessitates establishing NFET and PFET widths as $8w_{min}$ and $8K_{\mu}w_{min}$, respectively, where K_{μ} is defined as μ_n/μ_p in Equation (1), and W_{min} denotes the minimum transistor width.

$$K\mu = \mu_n / \mu_p (1)$$

where μ_n is the mobility of holes,

μ_p is the mobility of electrons and

W_{min} minimum transistor width

Excessively increasing the widths of NFET and PFET transistors escalates the layout area and power consumption. Yet, mitigating over-optimization in select layout components often proves complex without a means of controlling transistor sizing. Well-calibrated transistor sizing results in reduced delay and power consumption. In this study, we employ optimal sizing techniques to attain transistor dimensions that effectively curtail circuit delay and power dissipation. Different transistor sizes lead to varying input capacitances and output resistances, prompting standard cell libraries to encompass an array of cell sizes for each cell type.

The accomplishment of timing constraints hinges on selecting NFET and PFET widths tailored to distinct scenarios, optimizing rise and fall times. Optimal transistor sizing tangibly diminishes delay and power dissipation. Our work extends to crafting diverse N_Cell and P_Cell layouts based on optimal transistor dimensions. These are subsequently unified into NP cells, which play a pivotal role in reducing circuit layout area. Through integration of the NP-cell methodology with strategic transistor sizing, we achieve notable reductions in power consumption, delay, and layout area.

NP cells, exclusively composed of nfets and pfets, introduce heightened flexibility as they function akin to conventional cells. Although the positioning of NP cell instances is compatible with various placement algorithms, refined techniques are indispensable for instances that exhibit overlap. The overarching objective is to curtail overall layout area, while abiding by stipulated wire length ranges, maximal displacement thresholds, and precise alignment of N and P cell instances.

I. Design Methodology Of The Circuit

A. Overview

The design flow outlined in Figure 1 illustrates the systematic approach of the NP methodology. To achieve a notable reduction in delay and power dissipation within digital circuits, a multi-faceted strategy involving the manipulation of transistor sizes through various transistor sizing techniques is employed. In this study, our specific focus centers on the heuristic transistor sizing method, renowned for its efficacy. This process commences with the translation of given transistor specifications into practical transistor width values. This translation entails the utilization of critical parameters like threshold voltage and drain current, leading to a comprehensive parametric analysis. This analytical process culminates in the derivation of optimal transistor widths, a procedure replicated for both N-channel metal–oxide–semiconductor (Nmos) and P-channel metal–oxide–semiconductor (Pmos) transistors.

Extending this approach to encompass higher-level gates, such as NAND gates, ensures accurate sizing of pull-up and pull-down transistors. The resulting transistor dimensions are systematically tabulated alongside their corresponding delay and power characteristics. This meticulous sizing methodology stands as a testament to its efficacy, contributing significantly to the reduction in both delay and power dissipation across the designed digital circuits.

Subsequent to sizing optimization, the digital circuits are organized into discrete N_Cell and P_Cell entities. The integration of these distinct N_Cell and P_Cell instances serves as the cornerstone for the formation of NP_Cells—entities that encapsulate the comprehensive optimization philosophy. NP_Cells are strategically placed and routed to further streamline the layout area, concomitantly evaluating power and delay metrics to ensure holistic optimization benefits. This dynamic placement and routing procedure for N_Cell and P_Cell instances culminate in the creation of NP_Cells.

The execution of this methodology is facilitated by leveraging the Cadence Virtuoso tool, harnessed within the confines of the 90nm technology. The synthesis of heuristic transistor sizing, layout refinement through NP_Cell synthesis, and the intricacies of comprehensive placement and routing methodologies collectively contribute to the overarching objective of improving delay and layout area.

B. Transistor Sizing

The optimal design of circuits and instances hinges on the judicious sizing of transistors. In this pursuit, the heuristic transistor sizing approach emerges as a key strategy. Let's delve into the specifics of applying this technique to design an Inverter circuit, subsequently extending it to other circuit instances:

1. Inverter's Logical Behavior: The Inverter gate, a fundamental building block of digital circuits, exhibits a specific logic behavior. It produces a logic high output when fed a logic low input, and vice versa.

2. Technology Characteristics: Assuming a 90nm technology node, certain key characteristics are assumed, including a threshold voltage of around 0.5V for the transistors. Moreover, intrinsic capacitance is approximated at 1.2fF, with a standard gate-to-source voltage of 1.5V.

3. Load Capacitance Consideration: An important aspect of transistor sizing involves accounting for the load capacitance connected to the gate's output. For this scenario, a load capacitance of 1fF is assumed.

4. Drain Current Analysis: Delving into transistor behavior, the drain current characteristics are explored. This involves plotting the drain current against the Drain-to-Source voltage for a fixed Gate-Source voltage (1.5V) to understand the transistor's operational behavior.

5. Width Determination: With the drain current information in hand, the next step involves plotting the drain current against varying transistor widths. This aids in determining the optimal transistor width corresponding to desired drain current levels.

6. Applying Sizing to NMOS and PMOS: The sizing methodology, developed based on the Inverter's characteristics, is extended to both NMOS and PMOS transistors of the Inverter. This ensures a comprehensive approach to sizing.

By establishing the Inverter's transistor sizing, a robust foundation is laid for sizing subsequent circuits and instances. For instance, this paper extends the methodology to design NAND2 and D Flip-Flop (DFF) circuits, demonstrating the broad applicability of the approach. The designed circuits undergo rigorous analysis to assess their performance in terms of delay and power characteristics.

The crux of this study lies in the systematic application of heuristic transistor sizing, not only for individual transistors but also for complex circuitry. The incorporation of this methodology, coupled with meticulous design and analysis, substantiates the paper's central theme enhancing circuit efficiency through optimized transistor sizing and strategic circuit design.

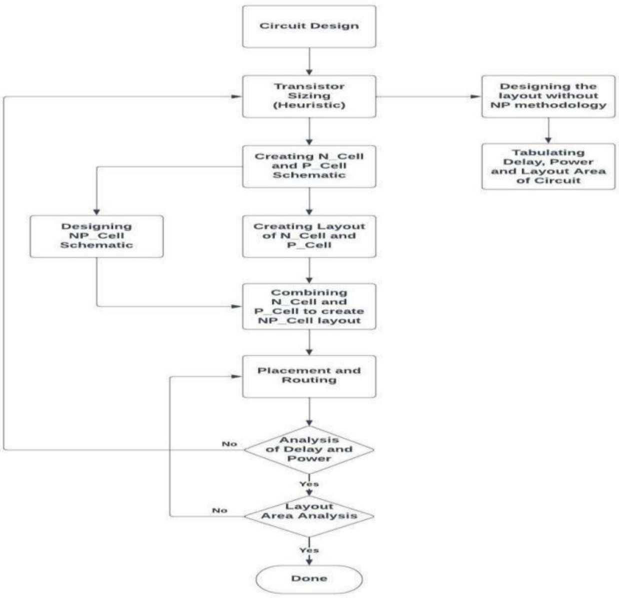

Figure.1 Design flow of NP methodology

C. NP Methodology

The Inverter's transistor dimensions are determined through the heuristic transistor sizing approach. This Inverter serves as the benchmark for sizing other circuits and instances. Specifically, this paper employs the same heuristic transistor sizing to design the NAND2 and D Flip-Flop (DFF) circuits. Building upon the transistor sizing procedure employed for the Inverter, the PMOS transistor is set at a width of 225nm, while the NMOS transistor measures 120nm.The sizing established for the Inverter serves as the foundation for the NAND2 circuit, where the pull-up transistor adopts a width of 225nm and the pull-down transistor is set at 240nm width. The sizing is meticulously applied to each pull-up and pull-down transistor, warranting individual schematic and layout design for both components.

Subsequently, the DFF circuit is constructed using the previously sized NAND2 gate. The corresponding N_Cell and P_Cell structures are generated for the NAND2 gate. Comprehensive delay and power analyses are conducted on these circuits, further extending to the measurement of the layout area for diverse DFF designs. Ensuring robustness in the design, meticulous placement and routing strategies are executed, conforming to clean Design Rule Checking (DRC) and Layout versus Schematic (LVS) procedures. For higher-level instance circuits, the placement and routing process benefits from optimized algorithms, facilitating efficient layout synthesis.

The detailed methodology, as showcased in Figure 1, encapsulates the step-by-step approach undertaken to design these circuits and instances. It is imperative to highlight the paper's emphasis on adherence to best practices in placement, routing, and layout synthesis, underscoring the meticulous attention to detail in achieving optimal circuit performance and efficiency gains.

II. Result And Discussion

Figure 2 offers a detailed view of the schematic for the NAND2 gate, an embodiment of the heuristic transistor sizing methodology utilized in alignment with the Inverter's specifications. Within this schematic, the pull-up transistor adheres to a width of 225nm, while the pull-down transistor assumes a width of 240nm.

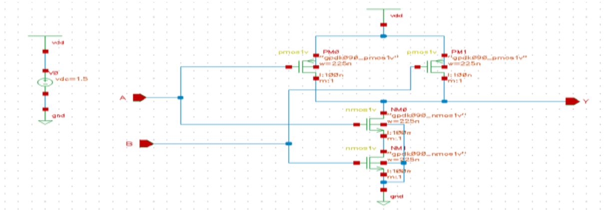

Figure.2 The schematic diagram of the NAND2

Transitioning to Figure 3, the simulation waveform for the NAND2 gate is presented. The delay and power metrics for both Pre-layout and Post-layout designs are meticulously gathered and recorded in Table 1.

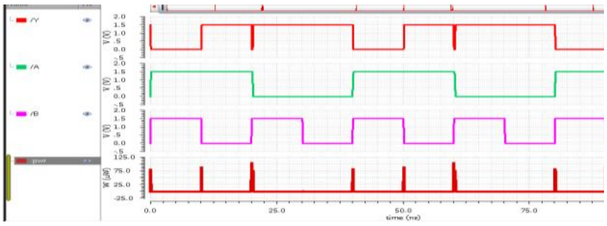

Figure.3 Simulation waveform of the NAND2

Figure 4 delves into the N_Cell and P_Cell aspects of the NAND2 gate. The P_Cell is designed with a width of 225nm, while the N_Cell dimensions stand at 240nm, maintaining coherence with the established sizing methodology.

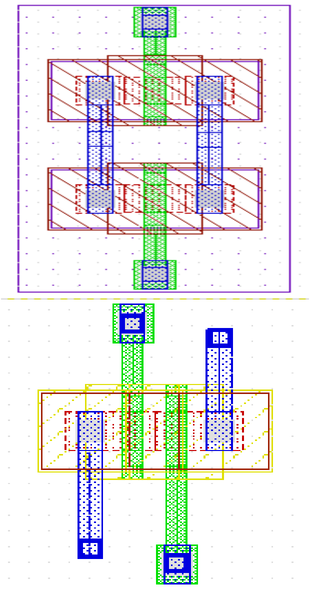

Figure.4 The P_Cell and N_Cell layout of the NAND2

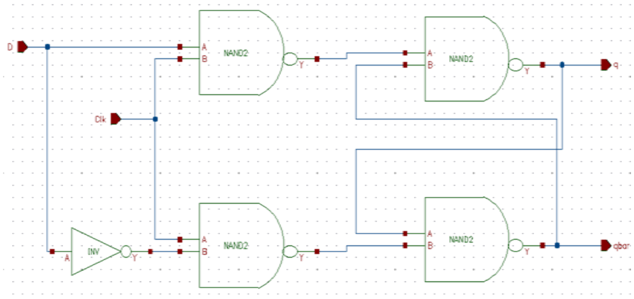

Figure.5 The schematic of the DFF

The subsequent focus, as demonstrated in Figure 5, is the schematic representation of the D Flip-Flop (DFF). This configuration employs four NAND2 gates and a single Inverter to achieve the desired DFF functionality.

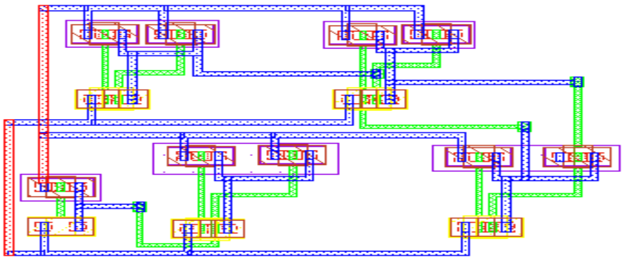

Figure.6 The layout of the DFF

Figure 6 and Figure 7 showcase the layout designs of the DFF circuit. The former layout is realized with NAND2 gates, while the latter employs the P_Cell and N_Cell structures derived from the NAND2 gate.

Figure 8 captures the simulation waveform of the DFF circuit.

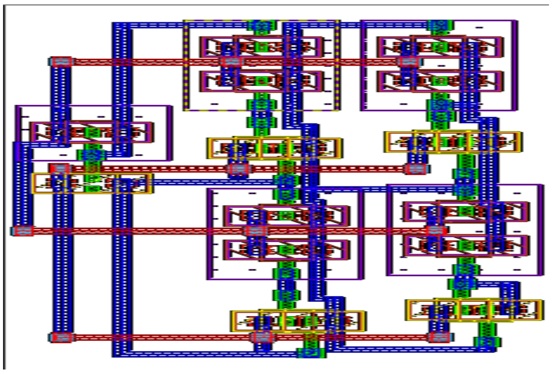

Figure.7 The layout of the DFF with NP

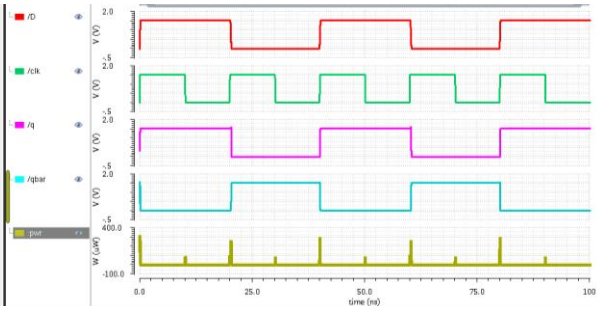

Figure.8 The simulation waveform of the DFF

Concluding this comprehensive analysis, the delay and power metrics of the DFF circuit are compiled and presented in Table 2. Additionally, the layout area for the DFF configurations is documented within the same table. This cohesive presentation encapsulates the intricate design process and subsequent analysis, underscoring the meticulous approach taken in assessing circuit behavior and performance.

The aforementioned figures and tables collectively depict the progression from schematic designs through simulation waveforms to layout configurations, while the tabulated data encapsulates the performance assessment of the designed circuits.

TABLE.1 The Delay and Power analysis of the circuit

	Delay		**Power(µW)**	
Gates/ Circuits	**Pre-Layout**	**Post-Layout**	**Pre-Layout**	**Post-Layout**
Inverter	8.431ps	8.846 ps	64.268	64.83
NAND2	35.8ps	36.45 ps	93.264	93.931
XOR2	9.87ns	10.09 ns	274.716	273.78
DFF	4.89ns	5.033 ns	316.497	316.43

TABLE.2 The Area analysis of the DFF

Circuits	**Without NP Methodology**	**With NP Methodology**
DFF	64.97m^2	41.33m^2
XOR2	68.46m^2	44.76m^2

III. **Conclusion**

In this paper, we have meticulously designed VLSI CMOS circuits, including an Inverter, two-input NAND gate, and D Flip-Flop, employing the highly effective Heuristic transistor sizing technique. The application of this approach has led to significant reductions in both delay and power dissipation across the circuits.Through the implementation of heuristic transistor sizing, we systematically constructed dedicated N_Cell and P_Cell structures for each of the designed componentsnamely, the Inverter, two-input NAND gate, and D Flip-Flop. Subsequently, the synergistic integration of these structures produced NP-Cells, which effectively combine the advantages of both N_Cell and P_Cell methodologies. This NP-Cell strategy proved instrumental in the design of complex circuits, such as the D Flip-Flop, showcasing the adaptability and scalability of this approach.

Comparative analyses of instances designed with and without the NP methodology have underscored its remarkable effectiveness. The introduction of NP-Cell technology consistently yielded reductions in layout area, reinforcing its ability to optimize layout efficiency. Moreover, the adoption of Heuristic transistor sizing yielded noteworthy improvements, resulting in gains of 4-15% in power efficiency and delay performance.The design of the D Flip-Flop and XOR2 gates using NP methodology demonstrated an impressive 34% reduction in layout area. This underscores the substantial area-saving potential inherent in the application of NP methodology.

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