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Fuzzy Sliding Mode Controller for Series Connected Solar Boost Inverter

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Abstract:
The paper develops a Fuzzy Sliding Mode Controller (FSMC) for improving the quality of power delivered to the load through two boost inverters connected in series from a Solar PV system. It includes a front end KY converter, which together with the capacitor offers a constant dc link voltage to the inverter. The framework evolves a rule based principle for engaging the gain of the FSMC to derive the reference, in an effort to modulate the pulse width modulation (PWM) pulses for the switches in both the inverters. The performance evaluated using MATLAB based simulation brings out the relative merits of the controller in terms of a lower total harmonic distortion (THD) and higher harmonic spread factor (HSF) for the output voltage of the inverter. It further exhibits the ability to ensure equal sharing of voltage among the inverters connected in series at the output and assuage to regulate the load voltage over the operating range. The experimental readings obtained from a prototype validate the simulation results and allows the claim for the use of the control strategy in similar practical systems.

Keywords: Series Boost Inverter, Fuzzy Proportional Integral (FPI), Fuzzy Sliding Mode Controller (FSMC), Total Harmonic Distortion (THD), Harmonic Spread Factor (HSF).

Introduction:

The inverter converts a dc voltage into an appropriate ac to support the connection of a power network or a load. The single stage boost inverter enables inverting and boosting or stepping up simultaneously the input dc voltage and finds widespread use in ac motor drives, uninterruptible power supplies (UPS) and renewable energy systems[1],

The boost type inverter referred to as the differential boost inverters achieves the dc-ac conversion through the differential connection of two dc-dc bidirectional boost sub converters [2]. Although the output voltage of each sub converter always remains positive, their ac components undergo a phase shift of 180 degrees and thus a sine wave with no dc offset may be provided to the differential load.

The conversion with two boost inverters connected in series offers a higher efficiency and reduction in the power rating besides being able to support high power applications [3]. The series inverter system allows in realizing low current and high voltage power supply, but however causes a higher voltage ripple in the modules which may degrade the output current. It inherits intrinsic redundancy, provides ride through capability and finds scope due to the limitation of power rating of switching device [4].

The series connection of the inverters due to the absence of high voltage devices and the use of the interleaving techniques significantly increase the equivalent frequency of the inductor because of which the switching frequency can be dramatically reduced and the efficiency further improved [5].

A large variety of configurations for the boost inverter have been suggested that include the H bridge inverter with step up transformer, Z source, fly back and buck boost inverter among others. However, the transformer or the inductor has been seen to increase the size of the inverter large because of the need for the heavy magnetic cores to sustain the higher output power. Besides the voltage stress of the switching device has been found to increase in high power applications [6].

The Z source inverter has been presented through a novel inverter topology with unique features and widely used especially in the PV field. It has been inherited with the ability to boost/buck the voltage using the Z source capacitor voltage and as a result increases the size and the weight of the system [7].

A new single phase closed loop Push Pull inverter, which provides both buck and boost voltage gain irrespective of the turns ratio of the transformer has been proposed. The turns ratio has been used to select the optimum operation of the inverter with regard to the degree of buck or boost and implemented by introducing a Z network between the dc source and the classical push pull inverter. The Z network whenever necessary has been engaged to boost up the voltage by going through the shoot through states and else operated in the normal PWM mode [8].

An interleaved buck converter, which steps down the input voltage, has been analyzed to explain in both the reduction of the output current and the current ripple amplitude. It has been seen to result in lowering the current stress of the components and the size of the output filter. The input voltages of the individual converters have been divided by the series connected capacitors and thus the step down ratio extended to reduce the voltage stress of the switches [9],

The conventional inverter has been integrated with the switched capacitors to offer a higher gain and efficiency, reduction in the voltage stress and improve the output voltage regulation. However, it has been experienced to face difficulties in relation to its control aspects [10].

A bidirectional buck boost inverter with SPWM control and an H bridge unfolding circuit has been explained as either a step down or step up inverter along with the electrolytic capacitors to lower the voltage rating. However, it has not been facilitated to compensate for the current harmonic distortion of a rectified load [11].

A new cascaded dual buck inverter has been brought out with the ability to be hard switched while utilizing the benefits of power MOSFETs at certain power levels. The voltage balancing of the two split capacitors in the topology has been necessitated to ensure the elimination of harmonics without which it has been seen to result in increased losses and decreased efficiency [12].

Problem Formulation

The primary target owes to design a FSMC for improving the quality of the output power from two boost inverters connected in series. It attempts to boost the voltage from the solar PV through suitable duty cycle changes to the KY converter. The formulation envisages deriving the appropriate reference from the gain values of the FSMC to modulate the PWM pulses and there from enable the enhancement to the power quality indices. The approach relates to investigating the performance both using simulation and experimental model with a view to establish the merits of the control scheme.

Proposed Strategy

The methodology orients to extract an ac output at the desired frequency and magnitude from a Solar PV source through the schematic explained using the Fig 1.

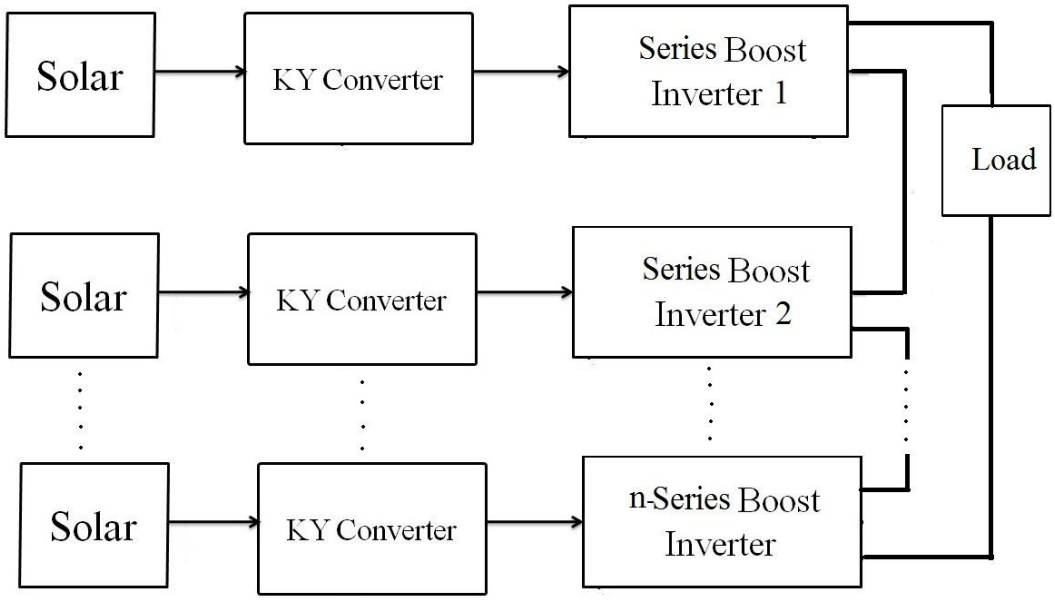

Fig. 1 Schematic Block Diagram

A PV module built by connecting many solar cells in series and parallel reflects the solar source where in a single solar cell can be modeled by utilizing a current source, a diode and two resistors. It enables the PV power to transform into electricity and may be estimated as the square of the current multiplied by the resistance of the circuit.

Unlike the traditional non isolated boost converter, the KY inherits fast transient load responses, similar to the behaviour of the buck converter. Besides, it produces non pulsating output current, thereby not only decreasing the current stress on the output capacitor but also reducing the output voltage ripple.

The circuit of the KY converter seen in the Fig. 2 consists of two switches S_1 and S_2 and a diode D for transferring energy to the capacitor C_b. It also includes an inductor L and Output capacitor C to ensure that the input voltage to the inverter remains constant.

The operation of the KY converter includes two modes where in the first mode, when S_1 turns ON, S_2 turn OFF and the voltage across L becomes equal to the sum of the input voltage and the voltage across C_b minus the output voltage vo, thereby causing L to be magnetized. It allows the energy available with C_b to be discharged and deliver power to the load. The current flowing through C turns out to be equal to the current i flowing through L minus the current flowing through R.

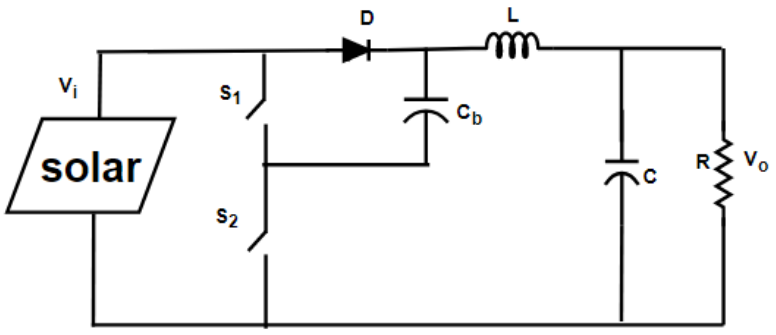

Fig. 2 Circuit Diagram of KY Converter

The switch S_1 turns OFF and S_2 turns ON during the second mode where in the voltage across L turns out to be equal to the input voltage v_i minus the output voltage v_o, thereby causing L to be demagnetized. The current flowing through C becomes equal to the current i flowing through L minus the current flowing through R. Besides, in this mode C_b abruptly charges to v_i within a very short time.

Modeling

The circuit topology of a boost inverter depicted in the Fig.3 inherits a structure based on a boost inverter that generates ac uni-polar ac output voltage and turns out to be higher than the input voltage It comprises N bidirectional boost converters connected in series with independent solar sources, and a resistive load is across the output.

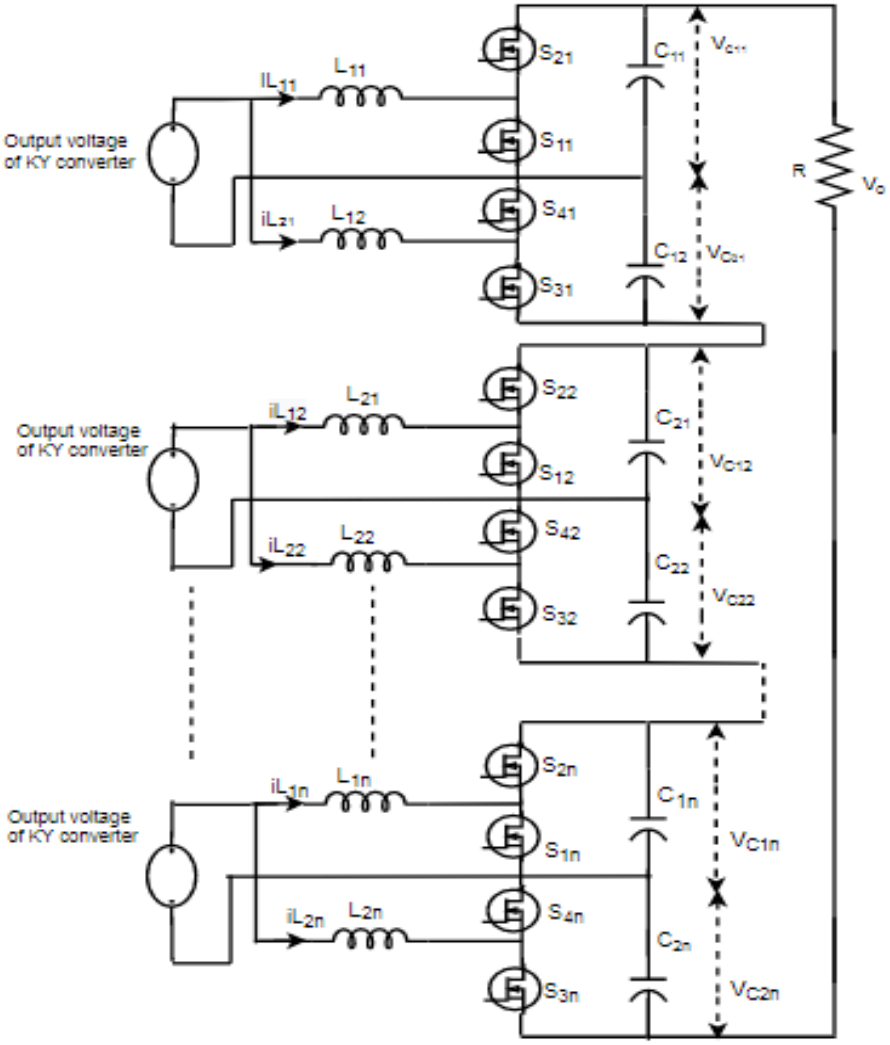

Fig. 3 Structure of Series Boost Inverter

The operation can be explained by considering the two modes with V_{in} being the input dc voltage. The circuit connects the inductances L_{11}, L_{12} ... L_{1n} and L_{21}, L_{22} ... L_{2n} in series with the semiconductor switches S_{11}, S_{12}... S_{1n}, S_{21}, S_{22} ... S_{2n}, S_{31}, S_{32} ... S_{3n} and S_{41}, S_{42} ... S_{4n}. The capacitors C_{11}, C_{12} ... C_{1n} and C_{21}, C_{22} ... C_{2n} connected across each boost inverter facilitate to create an 180 degree phase shift for the output voltage and R forms the load resistance respectively.

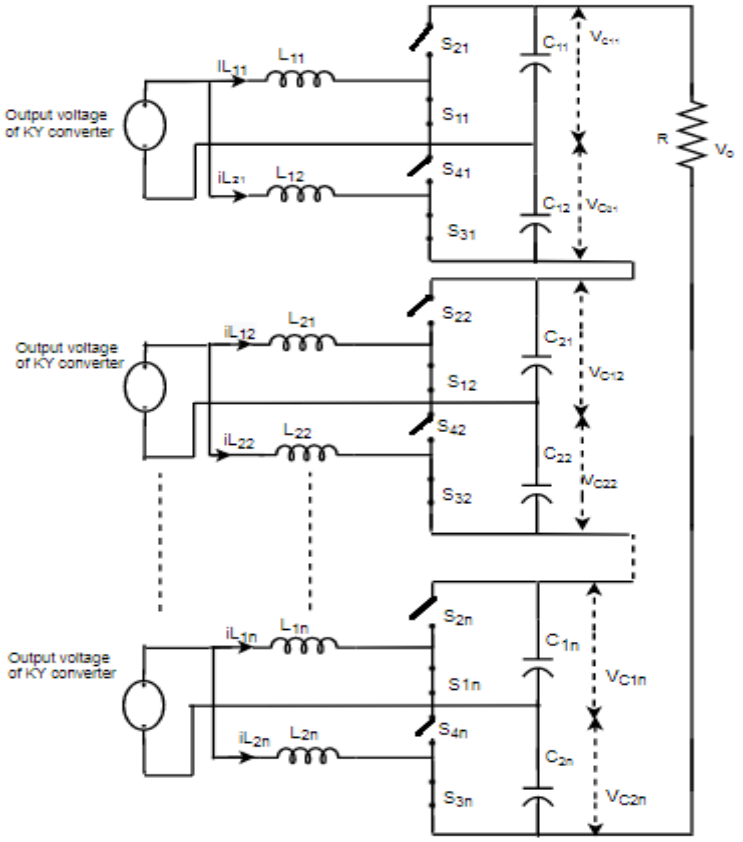

Fig. 4 Circuit diagram of Series Boost Inverter for Mode 1 Operation

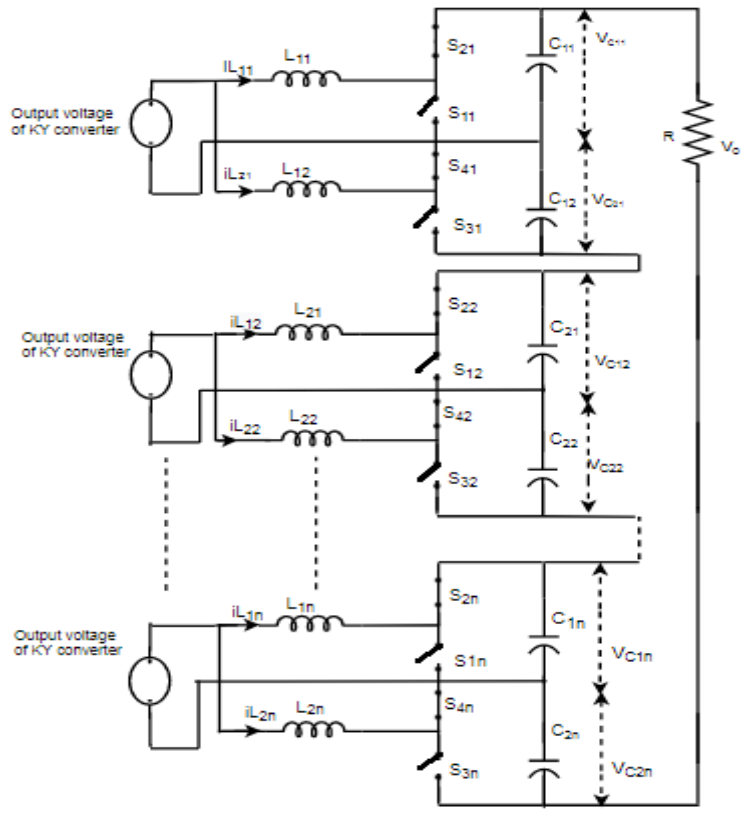

Fig. 5 Circuit diagram of Series Boost Inverter for Mode 2 Operation

The operation in the first mode reflected using the Fig. 4, enables the turning on of the switches S_{11}, S_{12} ....$S_{1n,}$ and S_{31}, S_{32}.... $S_{3n,}$ turning off of the switches S_{21}, S_{22} ... S_{2n} and S_{41}, S_{42} ... S_{4n}.While the inductor L_{11}, L_{12} ... L_{1n} charges, the inductor L_{21}, L_{22}... L_{2n} discharges and charges the capacitor C_{21}, C_{22}...$C_{2n.}$The capacitor C_{11}, C_{12} ... C_{1n} discharges to support the requirements of the load resistor R.

Similarly the theory in the second mode realized using the Fig. 5, where the switches S_{21}, S_{22} ... S_{2n} and S_{41}, S_{42} ... $S_{4n.}$ turn on and the switches S_{11}, S_{12} ....$S_{1n,}$ and S_{31}, S_{32}.... S_{3n} turn off. While the inductor L_{21}, L_{22} ... L_{2n} charges, the inductor L_{11}, L_{12}... L_{1n} discharges and charges the capacitor C_{11}, C_{12} ... C_{1n}. The capacitor C_{21}, C_{22} ... C_{2n} discharges and provides power to the load resistor R.

The state space model of series connected boost inverter can be derived by applying Kirchhoff's law to the circuit shown in the Fig. 4, as seen in the Eqns. [1] through [4].

$$\frac{di_{L_{1a}}}{dt} = \frac{V_{in}}{L_{1a}} \quad \text{---- (1)}$$

$$\frac{dv_{C_{1a}}}{dt} = \frac{-i_{L_{2a}}}{C_{1a}} \quad \text{---- (2)}$$

$$\frac{di_{L_{2a}}}{dt} = \frac{V_{in}}{L_{2a}} - \frac{V_{C_{2a}}`}{L_{2a}} \text{----- (3)}$$

$$\frac{dv_{C_{2a}}}{dt} = \frac{i_{L_{2a}}}{C_{2a}} - \frac{V_{C_{1a}}}{RC_{2a}} - \frac{V_{C_{2a}}}{RC_{2a}} \text{---- (4)}$$

The Eqn. (5) gives the general state space equation

$$\dot{\mathrm{X}} = \mathrm{AX} + \mathrm{BU} \quad (5)$$

Where $i_{L_{1a}}, i_{L_{2a}}, \mathrm{V_{C_{1a}}}, \mathrm{V_{C_{2a}}}$ represent the state variables

a = 1, 2, 3 ...n.

The state matrix of the system in the first mode may be expressed as in the Eqn. (6)

$$\begin{bmatrix} \frac{di_{L_{1a}}}{dt} \\ \frac{di_{L_{2a}}}{dt} \\ \frac{dV_{C_{1a}}}{dt} \\ \frac{dV_{C_{2a}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{L_{2a}} \\ 0 & \frac{-1}{c_{1a}} & 0 & 0 \\ 0 & \frac{1}{c_{2a}} & \frac{1}{RC_{2a}} & -\frac{1}{RC_{2a}} \end{bmatrix} \begin{bmatrix} i_{L_{1a}} \\ i_{L_{2a}} \\ V_{C_{1a}} \\ V_{C_{2a}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1a}} \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \end{bmatrix} V_{in} \quad \text{------ (6)}$$

On applying Kirchhoff's law to the inverter circuit in Fig. 5 gives the Eqns. (7) through (10)

$$\frac{di_{L_{1a}}}{dt} = \frac{V_{in}}{L_{1a}} - \frac{V_{C_{1a}}}{L_{1a}} \text{----- (7)}$$

$$\frac{dv_{C_{1a}}}{dt} = \frac{iL_{1a}}{C_{1a}} \quad \text{------ (8)}$$

$$\frac{di_{L_{2a}}}{dt} = \frac{V_{in}}{L_{2a}} \text{------- (9)}$$

$$\frac{dv_{C_{2a}}}{dt} = \frac{-i_{L_{1a}}}{C_{2a}} - \frac{V_{C_{1a}}}{RC_{2a}} - \frac{V_{C_{2a}}}{RC_{2a}} \text{---- (10)}$$

The state matrix of the system relating to the second mode can be written as in the Eqn. (11)

$$\begin{bmatrix} \frac{di_{L_{1a}}}{dt} \\ \frac{di_{L_{2a}}}{dt} \\ \frac{dV_{C_{1a}}}{dt} \\ \frac{dV_{C_{2a}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_{1a}} & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{c_{1a}} & 0 & 0 & 0 \\ \frac{-1}{c_{2a}} & 0 & \frac{-1}{RC_{2a}} & -\frac{-1}{RC_{2a}} \end{bmatrix} \begin{bmatrix} i_{L_{1a}} \\ i_{L_{2a}} \\ V_{C_{1a}} \\ V_{C_{2a}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1a}} \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \end{bmatrix} V_{in} \quad \text{------ (11)}$$

Using the state space averaging technique, the final state matrix may be represented as in the Eqn. (12)

$$\begin{bmatrix} \frac{di_{L_{1a}}}{dt} \\ \frac{di_{L_{2a}}}{dt} \\ \frac{dV_{C_{1a}}}{dt} \\ \frac{dV_{C_{2a}}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{-(1-D)}{L_{1a}} & 0 \\ 0 & 0 & 0 & \frac{-D}{L_{2a}} \\ \frac{(1-D)}{c_{1a}} & \frac{-D}{C_{1a}} & 0 & 0 \\ \frac{-(1-D)}{c_{2a}} & \frac{D}{C_{2a}} & \frac{-1}{RC_{2a}} & -\frac{-1}{RC_{2a}} \end{bmatrix} \begin{bmatrix} i_{L_{1a}} \\ i_{L_{2a}} \\ V_{C_{1a}} \\ V_{C_{2a}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{1a}} \\ \frac{1}{L_{2a}} \\ 0 \\ 0 \end{bmatrix} V_{in} \text{-------- (12)}$$

Control Algorthim

The function of the inverters mainly involves a satisfactory delivery of power to ac loads and the modulation strategy therefore plays a crucial role in determining the performance of the system. Apart from complying with the performance factors, the issues relating to modifying the control parameters do play a significant role.

The terms relating to both the current and voltage appear in the modeling equations, which however may make it difficult to control the output voltage for the boost inverter. Besides with the PI controller the presence of zero dynamics with respect to the output voltage may create instability to the system. Therefore the choice of introducing an intelligent controller together with the traditional methods allows extracting better results in terms of improving the quality of power received by the load.

The philosophy of the fuzzy logic controller (FLC) relies on the fuzzy inference mechanism and does not require a mathematical model for controlling the system. The design of the FLC orients to obtain the feedback control gain from the inference rule base. The fuzzy sliding mode control systems design engages the assumption that the system states remain available for measurement and may be formulated as functions of the tracking error for the system with the error and the derivative of the error as inputs.

There exists a switching line along the diagonal of the fuzzy logic rule table and the control signal inherits opposite signs at the two sides of the diagonal. When the system states lie far away from the diagonal, it becomes big and vice versa used with the sliding function as input and the control force as output in the controller. The fuzzy control rules for the error and change of error can be referred in the Table. 1 and the output may be obtained through the weighted average of consequents.

Table. 1Fuzzy Rule base

Change in fuzzy Δ F		Change in Error (Δe)						
		NB	NM	NS	ZE	PS	PM	PB
Error (e)	NB	NB	NB	NB	NB	NM	NS	ZE
	NM	NB	NB	NB	NM	NS	ZE	PS
	NS	NB	NB	NM	NS	ZE	PS	PM
	ZE	NB	NM	NS	ZE	PS	PM	PB
	PS	NM	NS	ZE	PS	PM	PB	PB
	PM	NS	ZE	PS	PM	PB	PB	PB
	PB	ZE	PS	PM	PB	PB	PB	PB

The Fig. 6 represents the block diagram of the boost inverter with the introduction of the fuzzy sliding mode controller (FSMC) for tuning the sliding surface. The terms Vref and V_o refer to the reference and the output voltage respectively.

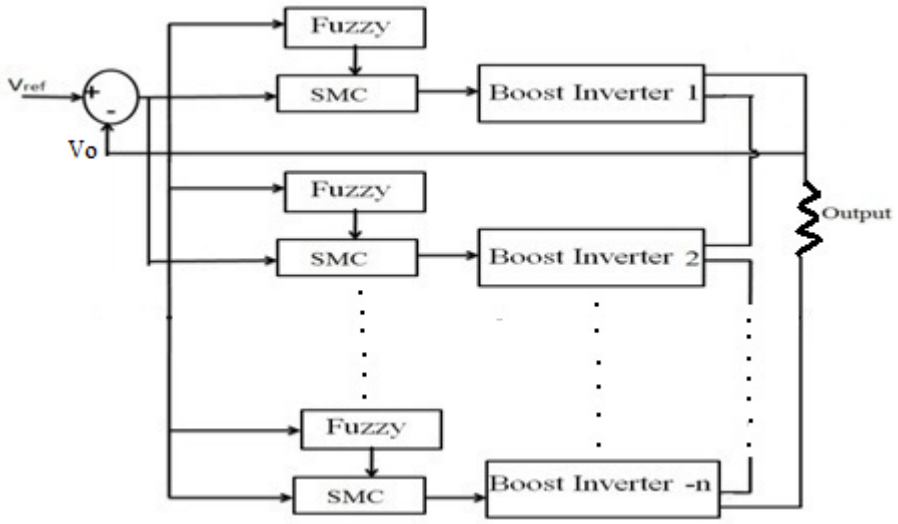

Fig.6 Series Boost Inverter with FSMC

The control variable X may be expressed in the general form as in the Eqn. (13)

$$X = \begin{bmatrix} X_1 \\ X_2 \\ X_3 \end{bmatrix} = \begin{bmatrix} v_{ref} - \beta v_o \\ \frac{d(V_{ref} - \beta V_0)}{dt} \\ \int v_{ref} - \beta v_o \end{bmatrix} \text{------ (13)}$$

where X_1, X_2, and X_3 represent the voltage error, the voltage error dynamic (or the rate of change of voltage error), and the integral of voltage error individually.

The Eqns. (14) to (16) may be obtained from (13)

$$X_1 = V_{ref} - \beta V_o \text{ ------- (14)}$$

$$\dot{X}_1 = \frac{d(V_{ref} - \beta V_o)}{dt} = X_2 \text{ -------- (15)}$$

$$\mathrm{X_2} = -\beta \frac{\mathrm{dV_o}}{\mathrm{dt}} \text{ ------ (16)}$$

where V_o refers to the load voltage,
V_{ref} - Reference voltage.
β - Sensed output voltage.

The rate of change of the output voltage may be expressed as in the Eqn. (17)

$$\frac{dv_0}{dt} = \left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} - \frac{V_0}{RC_{2a}} \text{ ------- (17)}$$

The expression in the Eqn. (18) can be obtained from the Eqn. (7)

$$\mathrm{i_{L_{1a}}} = \int \frac{\mathrm{V_{in} - V_{C_{1a}}}}{\mathrm{L_{1a}}} \overline{\mathrm{u}} \mathrm{dt} \text{ ------ (18)}$$

The control variable X_2 in the Eqn. (19) may be deduced by substituting the Eqn. (17) and Eqn.(18) in the Eqn. (16)

$$X_2 = -\beta \left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] \int \frac{\mathrm{V_{in} - V_{C_{1a}}}}{\mathrm{L_{1a}}} \overline{\mathrm{u}} + \beta \frac{V_o}{RC_{2a}} \text{ ----- (19)}$$

$$X_3 = \int (V_{ref} - \beta V_o)\ dt \text{ ------- (20)}$$

The control variable X in Eqn.(13) thus becomes

$$X_{boost} = \begin{bmatrix} v_{ref} - \beta v_o \\ -\beta \left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] \int \frac{\mathrm{V_{in} - V_{C_{1a}}}}{\mathrm{L_{1a}}} \overline{\mathrm{u}} + \beta \frac{V_o}{RC_{2a}} \\ \int v_{ref} - \beta v_o \end{bmatrix} \text{ ------ (21)}$$

where $\overline{u}$ =1- u refers to the inverse logic of u.

The time differentiation of the Eqn. (21) produces the state space description in the Eqns. (22), (23) and (24)

$$\dot{X}_1 = \frac{d}{dt}\left(v_{ref} - \beta v_o\right) = X_2 \text{ ---- (22)}$$

$$\dot{X}_2 = -\beta \left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] \frac{\mathrm{V_{in} - V_{C_{1a}}}}{\mathrm{L_{1a}}} \overline{\mathrm{u}} - \frac{1}{RC_{2a}} X_2 \text{ ---- (23)}$$

$$\dot{X}_3 = v_{ref} - \beta v_o = X_1 \text{ ---- (24)}$$

The Eqn. (22) through (24) may be expressed in the matrix form as in the Eqn. (25)

$$\begin{bmatrix} \dot{\mathrm{X}}_1 \\ \dot{\mathrm{X}}_2 \\ \dot{\mathrm{X}}_3 \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -1/RC_{2a} & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \mathrm{X}_1 \\ \mathrm{X}_2 \\ \mathrm{X}_3 \end{bmatrix} + \begin{bmatrix} 0 \\ -\beta \left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] \frac{\mathrm{V_{in} - V_{C_{1a}}}}{\mathrm{L_{1a}}} \\ 0 \end{bmatrix} [\overline{u}] \text{ ------ (25)}$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & -1/RC_{2a} & 0 \\ 1 & 0 & 0 \end{bmatrix} \qquad B = \begin{bmatrix} 0 \\ -\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}} \\ 0 \end{bmatrix}$$

The overall sliding mode control law that generates the switching function can be written as in the Eqn. (26)

u = 1when S > 0

= 0 when S < 0 ------- (26)

where S relates to the instantaneous state variable trajectory and described as in the Eqn. (27)

$$S = (\alpha_1 X_1 + \alpha_2 X_2 + \alpha_3 X_3) = J^T X \text{ ------ (27)}$$

where $J^T = [\alpha_1, \alpha_2, \alpha_3]$ and $\alpha_1, \alpha_2, \alpha_3$ represent the control parameters termed as sliding coefficients. The equivalent control signal $u_{eq.}$ which reflects the smooth capacity of the discrete input function u, defined as utilizing the invariance conditions by setting the time differentiation of the Eqn. (27) as $\dot{S} = 0$. The equivalent control function enables the determination of the duty cycle in the form of a pulse to the switches in both the inverters.

Equating $\dot{S} = J^T AX + A^T B\overline{u}_{eq} = 0$ yield the equivalent control function in the Eqn.(28), which on being simplified through the Eqns. (29) to (31) gives the final form as in the Eqn. (32)

$$\overline{u}_{eq} = -[J^T B]^{-1} J^T AX \text{ ------ (28)}$$

$$-J^T B = \alpha_2\left[-\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right] \text{----- (29)}$$

$$J^T AX = \alpha_3(V_{ref} - \beta V_0) - \beta\left(\alpha_1 - \frac{\alpha_2}{RC_{2a}}\right)\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} + \frac{\beta V_o}{RC_{2a}}\left(\alpha_1 - \frac{\alpha_2}{RC_{2a}}\right) \text{ ----- (30)}$$

$$\overline{u}_{eq} = \frac{\alpha_3(V_{ref}-\beta V_0) - \beta\left(\alpha_1 - \frac{\alpha_2}{RC_{2a}}\right)\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} + \frac{\beta V_o}{RC_{2a}}\left(\alpha_1 - \frac{\alpha_2}{RC_{2a}}\right)}{\alpha_2\left[\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right]} \text{ ----- (31)}$$

$$\overline{u}_{eq} = \frac{1}{\left[\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right]}\left[\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_0) - \beta\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right)\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} + \frac{\beta V_o}{RC_{2a}}\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right)\right] \text{ ---- (32)}$$

where the control variable $\overline{u}_{eq}$ may be a continuous function and vary between $0 < \overline{u}_{eq} < 1$ as an inequality constraint, which on being substituted in the Eqn. (32) gives rise to the Eqn.(33).

$$0 < u_{eq} = 1 - \left[\frac{1}{\left[\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right]}\left[\frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_0) - \beta\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right)\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} + \frac{\beta V_o}{RC_{2a}}\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right)\right]\right] < 1 \text{ ----}$$

-- (33)

Multiplying the inequality function in the Eqn. (33) by $\left[\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right]$ gives the Eqn. (34)

$$0 < u_{eq} = \left[\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right] - \frac{\alpha_3}{\alpha_2}(V_{ref} - \beta V_0) + \beta\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right)\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} - \frac{\beta V_o}{RC_{2a}}\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right) < \beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}} \text{ --- (34)}$$

The equivalent control function in the Eqn. (27) may be related to the duty ratio control d, where 0 < d = $\frac{v_c}{v_{ramp}}$ < 1 as in the Eqn. (35) and there from arrives at the expression for the control signal V_C and ramp signal V_{ramp} in the Eqns. (36) and (39). The Eqns. (37) and (38) refer to the constants in the Eqn. (36)

$$V_c = U_{eq} = \left[\beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}}\right] - \frac{\alpha_3}{\alpha_2}\left(V_{ref} - \beta V_0\right) + \beta\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right)\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] i_{L_{1a}} - \frac{\beta V_o}{RC_{2a}}\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right) \text{---- (35)}$$

$$V_c = V_{ramp} - K_{p2}\left(v_{ref} - \beta v_o\right) + K_{p1}\left[i_{L_{1a}}\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right] - \frac{V_o}{RC_{2a}}\right] \text{---- (36)}$$

$$K_{p2} = \left(\frac{\alpha_3}{\alpha_2}\right) \text{----- (37)}$$

$$K_{p1} = \beta\left(\frac{\alpha_1}{\alpha_2} - \frac{1}{RC_{2a}}\right) \text{----- (38)}$$

$$V_{ramp} = \beta\left[\frac{1}{C_{2a}} - \frac{1}{C_{1a}}\right]\frac{V_{in}-V_{C_{1a}}}{L_{1a}} \text{----- (39)}$$

Simulation Results:

The procedure involves evaluating the performance of the two boost inverters connected in series at the output through simulation on the MATLAB/ Simulink platform. The identically rated inverters comprise elements that include L_{1a} = L_{2a} =10mH, capacitance C_{1a} = C_{2a} = 95µF, switching frequency Fs= 50 kHz and the load resistance allowed to vary upto 1kW. It operates from a system of series connected solar panels supported through a dc-dc based KY converter and the Tables. 2 and 3 include their respective specifications.

Table .2 Solar Specifications

PV Module		PV Array	
Number of cells in a modules	72	Voltage at MPP, Vmpp =Vpv	166.5V
Open circuits voltage	22.32V	Power at MPP, Pmpp = Ppv	2250W
Short circuit current	14.50A	Current at MPP, Impp = Ipv	13.5A
Voltage at MPP, V_m	18.50V	No. of Series Modules Ns	V_{amp}/V_{im}=9
Current at MPP, I_m	13.52A	No. of Parallel Modules Np	I_{mp}/I_m=1

Table. 3
Specification of KY Converter

Description	Parameter	Nominal Voltage
Input Voltage	V_i	72.36
Desired Output Voltage	V_o	100
Capacitor	C	100µF
Inductor	L	15µH
Switching frequency	f_s	50KHz

The total open circuit voltage of the solar being rated for 72 Volts finds the output voltage of the KY to be 100V and enables an output of 115 Volts at the output of the each inverter to provide 230 Volts to the load.

It maintains a constant dc link voltage through duty cycle changes to the KY converter, in addition to its attempts to lower the ripple in the voltage. The introduction of the fuzzy tuned SMC enables equal sharing of the voltage between the two series connected inverters and regulates the load voltage across the operating range. The FSMC encompasses with it measures to improve the quality of the power delivered to the load through a reduction in the THD and an increase in the HSF of the output voltage over the range of operating loads.

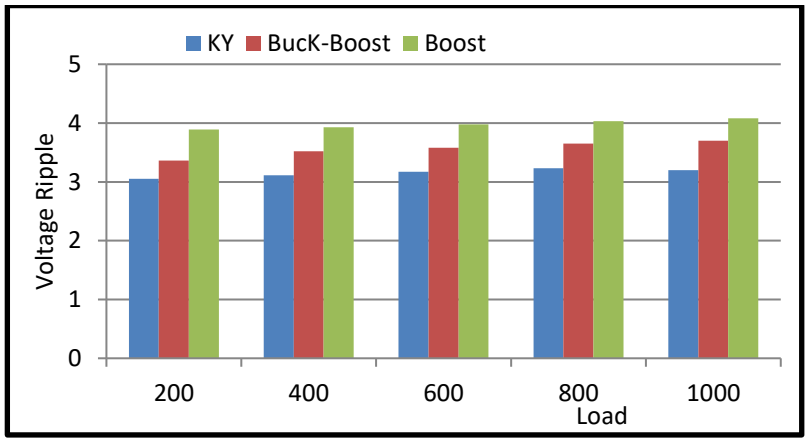

Fig 7: Voltage Ripple of the Converter

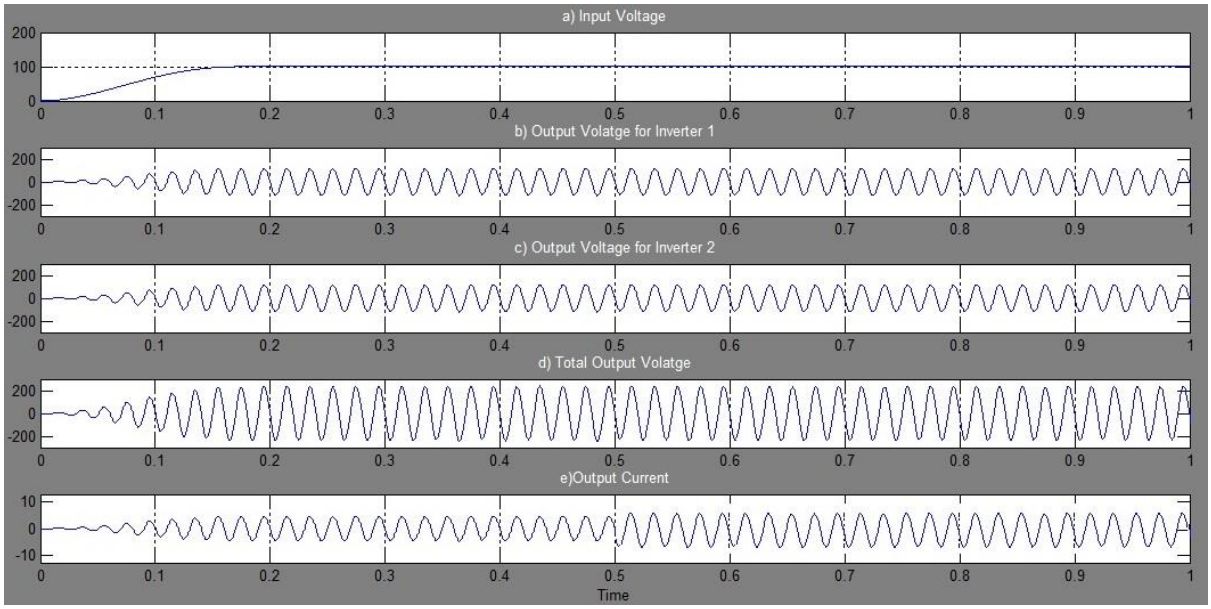

Fig. 8 Steady State and Regulatory response for FSMC

The bar diagram in the Fig.7 depicts the ripple in the dc link voltage expressed in percentage as a function of the different values of the operating loads. It brings out that the KY converter enjoys a lower ripple than the conventional boost converter owing to the filtering presence of two inductors and capacitors in the KY converter.

The Fig. 8 relates to the regulated dc link voltage, the output voltage of the two inverters, the regulated load voltage and the output current corresponding to a load power of 1kW using FSMC.

The plots exhibit the ability of the FSMC strategy to ensure equal sharing of the voltage among the two inverters and regulate the load voltage across the operating range.

The fuzzy tuned SMC further allows rejection of the load disturbance in the sense on being subjected to a sudden increase in load by 10 percent at 0.5 seconds respectively, though the output current raises correspondingly, the load voltage remains regulated.

The THD measured using the FFT spectrum for the load voltage and the inverter current at the same operating point in the Figs 9 through 12 reflect the benefits of the FSMC in terms of a lower THD than the FPI controller. The bar chart in the Figs. 13 and 14 compare the output voltage and the input current THD obtained using the FSMC and FPI controllers for the range of operating loads and further claim the merits of the FSMC over the FPI controller. Similarly the values of the HSF drawn for the load voltage using the bar diagram in the Fig.15 across the operating range justify the use of the FSMC.

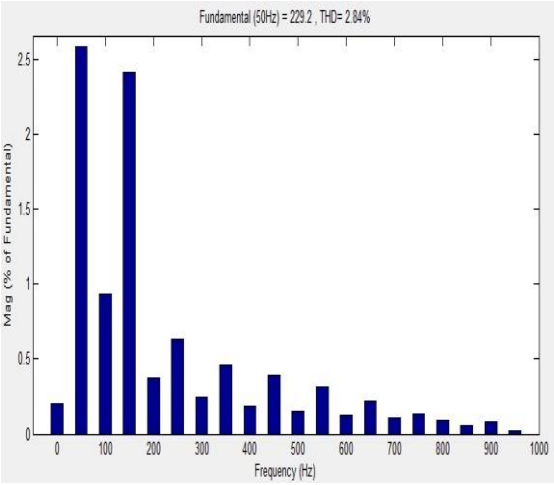

Fig 9: Voltage THD in FSMC

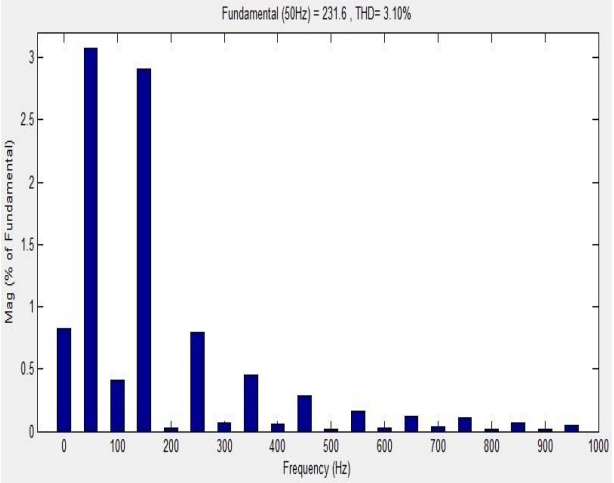

Fig 10: Voltage THD in FPI

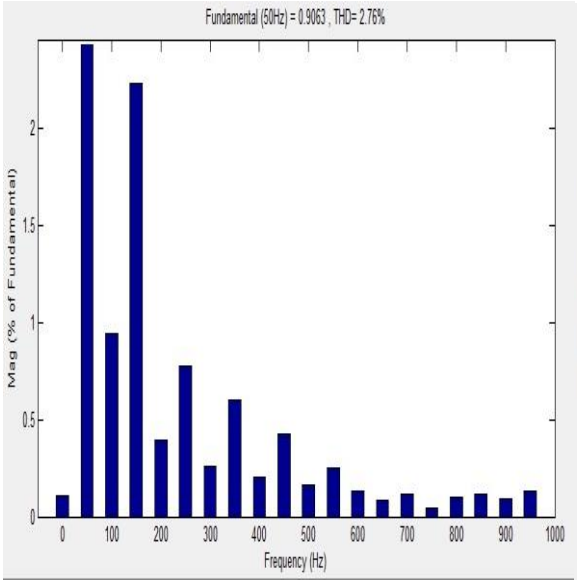

Fig. 11 Current THD in FSMC

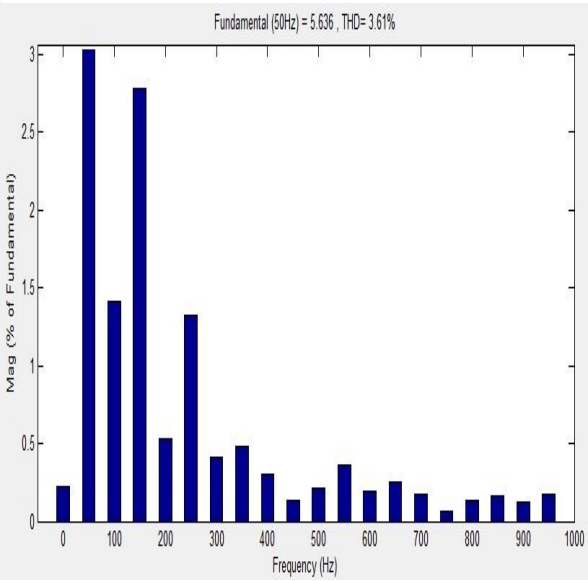

Fig. 12 Current THD in FPI

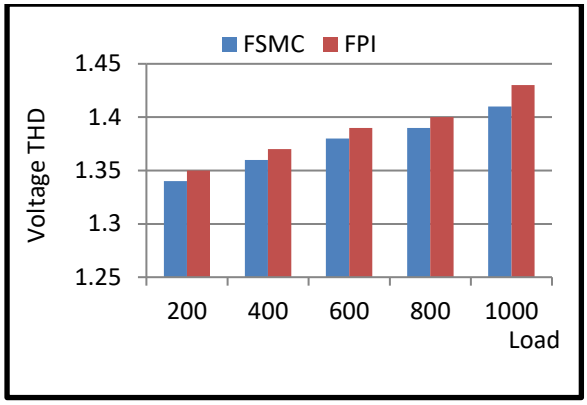

Fig 13: Output Voltage THD

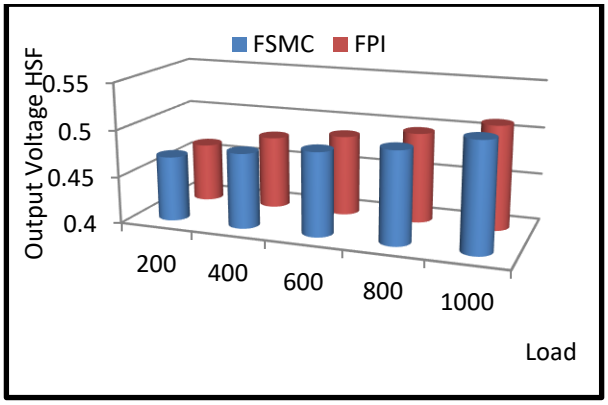

Fig 15: HSF of Inverter Output Voltage

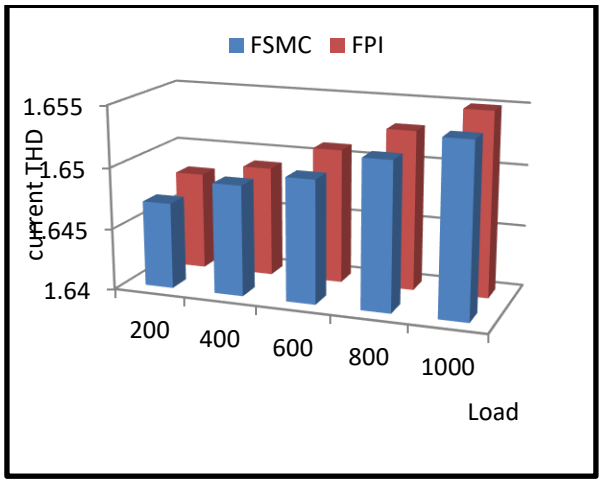

Fig 14: Inverter Current THD

Hardware Implementation:

The methodology involves the use of an Atmega processor to generate the PWM pulses for the MOSFET switches in accordance with the design of the control strategy. The ATmega belongs to a class of single chip microcontroller created by Atmel in the mega AVR(**A**lf and **V**egard's **R**ISC processor) family (later Microchip Technology acquired Atmega in 2016).

The Atmel ATmega8 combines an 8 bit RISC CPU with In System Self Programmable Flash on a monolithic chip to be a powerful microcontroller that provides a highly flexible and cost effective solution for many embedded control applications. It allows to be supported with a full suite of program and system development tools, including C compilers, macro assemblers, program simulators, and evaluation kits. It includes an 8 KB Program memory (Flash Memory) for storing the programming code and permanent settings. Besides it comes with an EEPROM memory of 512 bytes and a RAM memory of 1KB for being refreshed on restarting. A power up timer, a watchdog timer, Brown out Detection, In Circuit Serial Programming and five sleep modes form part of the other features in the processor. .

The device manufactured using Atmel's high density non volatile memory technology enables the Flash Program memory to be reprogrammed In System through an SPI serial interface using either a conventional non volatile memory programmer or by an On chip boot program running on the AVR core. The boot program can use any interface to download the application program in the Application Flash memory.

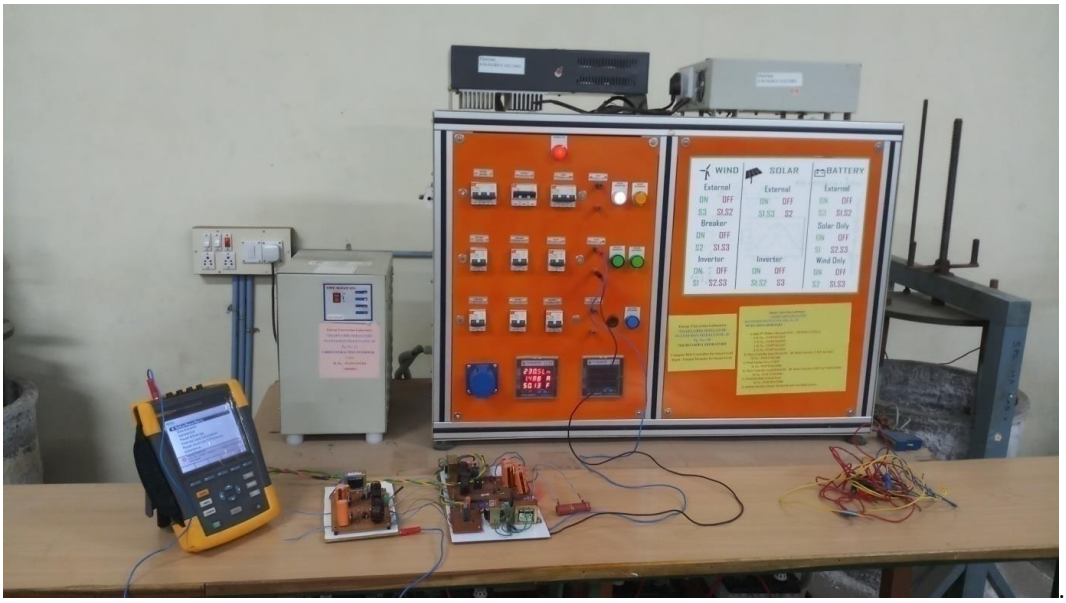

Fig 16 Prototype

The exercise extends to study the performance of the control schemes using an experimental prototype seen in the Fig.16 with similar ratings as that used in simulation. It operates from the solar source controlled using a battery charger with the KY converter and deliver power to the resistive load. The Fig. 17 outlines the flow schematic involving the generation of appropriate firing pulses for the MOSFET switches in the two inverters.

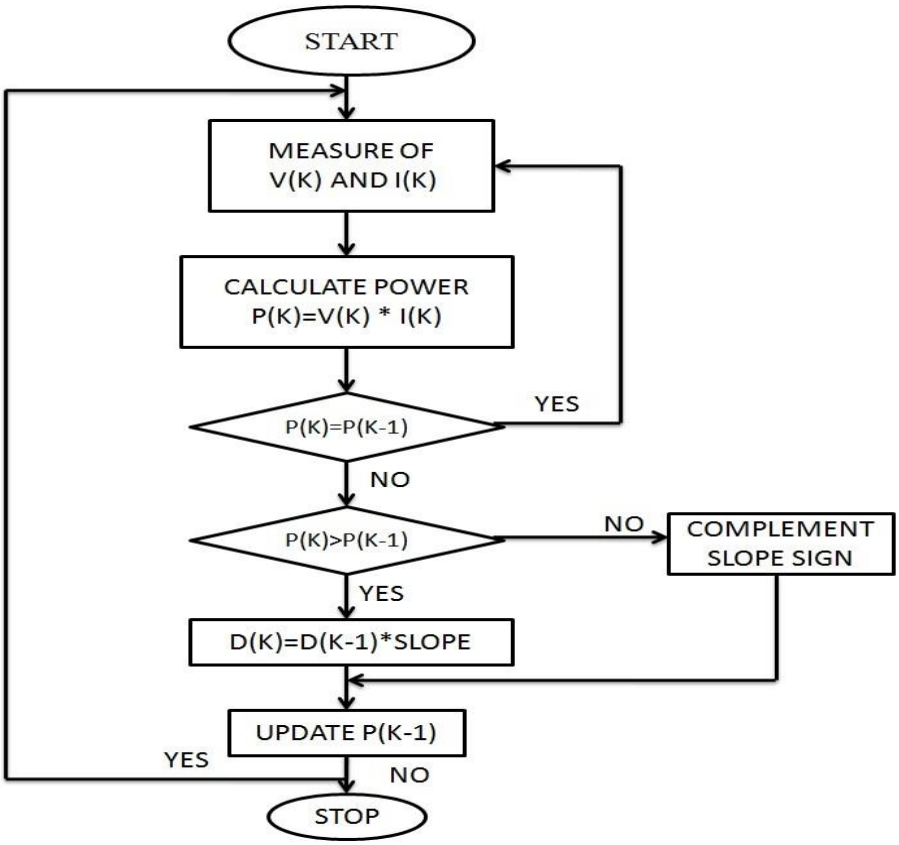

Fig 17 Flow Chart

The Table 4 compares the results of the FPI and FSMC for various values of load power to bring out that the superiority of the FSMC. The Fig 18 through 21 showcases the pulses to the switches in the inverter, the output voltage, the load current and the voltage THD spectrum corresponding to an operating point of 1 kW reflects the benefits of the inverter and the efficiency of the control algorithm.

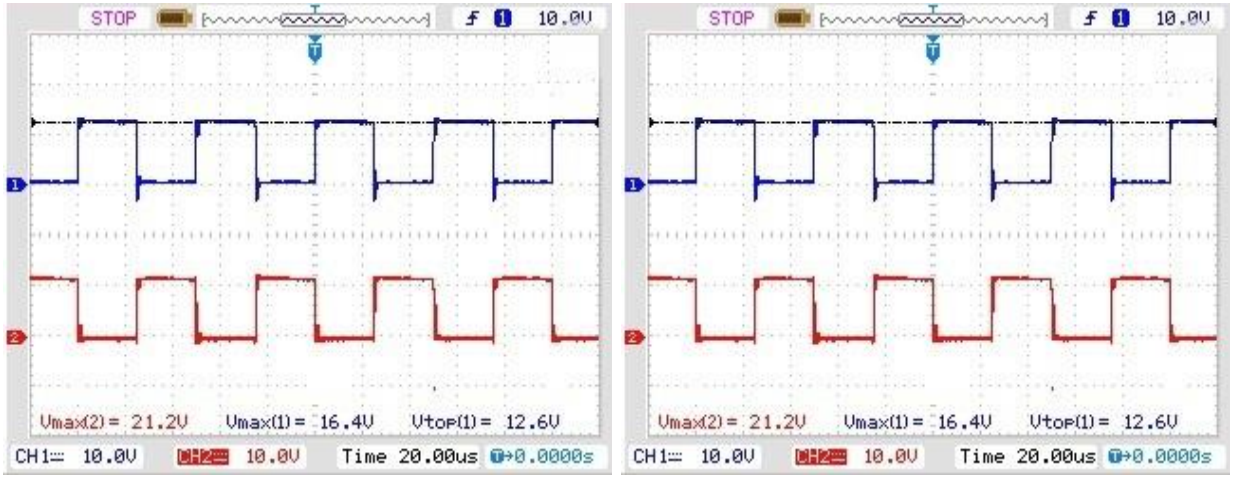

Fig. 18 PWM Pulses to Inverter Switches

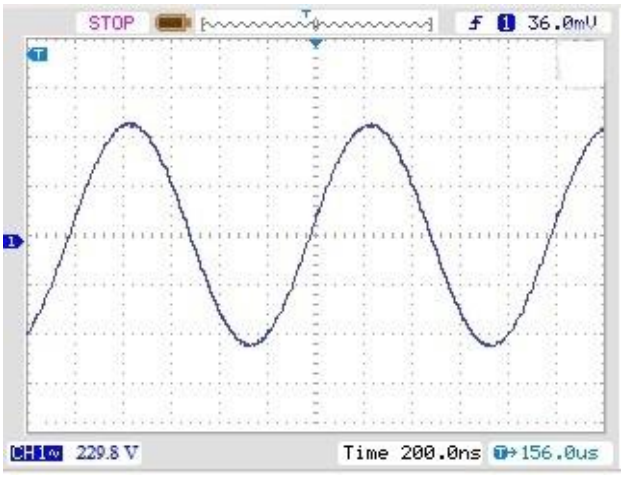

Fig 19: Output Voltage of Inverter

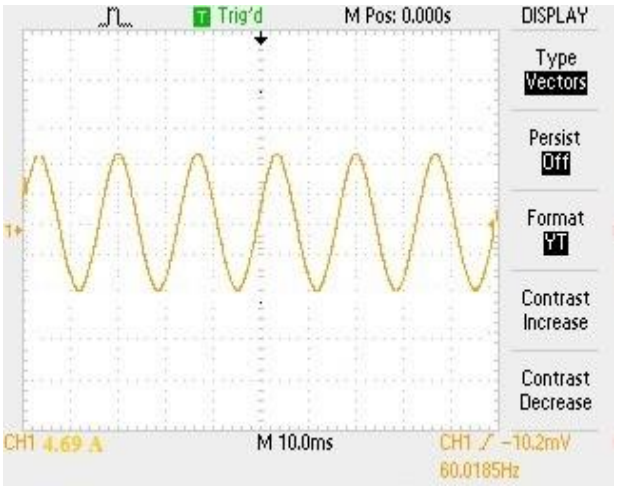

Fig 20: Output Current of Inverter

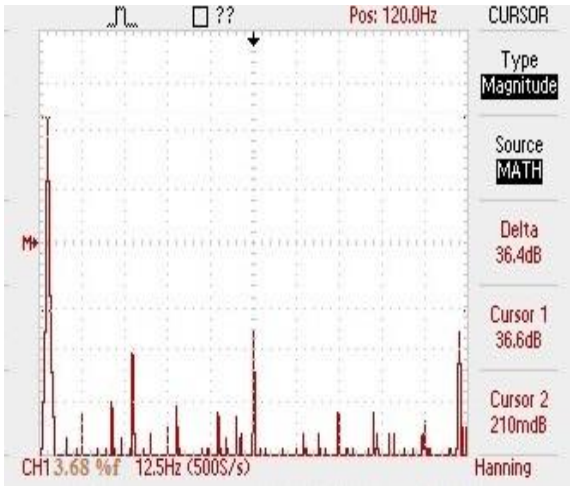

Fig 21: Output Voltage THD

Table 4
Performance Comparisons

Load in watts	Output voltage of K converter (V)	Output Voltage for Inverter 1 (V)			Output Voltage fo Inverter 2 (V)			Total Output Voltage (v)			Output Current (A)			Load Voltage THD		
		FSMC	FPI	Hard Ware	FSM	FPI	Hard Ware	FSMC	FPI	Hard ware	FSMC	FPI	Hard ware	FSM	FPI	Hard ware
200	100.2	115.1	115.7	117	115.	115.7	117	230.2	231.4	234	0.86	0.86	0.9	1.34	1.35	1.42
400	100.1	115.0	115.6	116	115.	115.6	116	230.1	231.2	232	1.73	1.73	1.8	1.36	1.37	1.46
600	100.0	114.9	115.2	115	114.	115.2	115	229.8	230.4	230	2.61	2.60	2.7	1.38	1.39	1.48
800	99.9	114.8	114.9	115	114.	114.9	115	229.6	229.8	230	3.48	3.47	3.5	1.39	1.40	1.52
1000	99.7	114.7	114.8	114	114.	114.8	114	229.4	229.6	228	4.35	4.36	4.4	1.41	1.43	1.58

Conclusion:

A FSMC based methodology suitable for solar boost inverters has been developed to enable uniform sharing of output voltage among the inverters connected in series in addition to regulating its load voltage. The design of the fuzzy based controllers have been elicited to derive appropriate reference signals for generating the PWM pulses to the switches in the inverters which in turn facilitates to realize a better quality of power delivered to the load. The simulation results have been portrayed to justify the choice of the KY converter through its ability to reduce the voltage ripple and maintain a constant voltage to the inverters. The close comparison of the experimental and simulation readings have been fostered to allow the use of the series connection of the inverters with a view to reduce the voltage stress for the switches in practice. The outcomes have been illustrated to guarantee the merits for the FSMC and claim the use of the control scheme in similar applications.

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