Journal of Harbin Engineering University
ISSN: 1006-7043

Vol 45 No. 9
September 2024

Enhancing Block Level Performance with CTS Optimization for High-Frequency Nodes in SOC

[1] Kokila S, [2] Dr. Srividya P

Department of Electronics and Communication Engineering

[1] Student, RV College of Engineering, Bangalore

[2] Associate Professor, RV College of Engineering, Bangalore

Abstract

In the realm of Very-Large-Scale Integration (VLSI) circuit design, achieving optimal performance in System-on-Chip (SoC) architectures for high-frequency nodes presents significant challenges. As semiconductor technology advances, the demand for higher performance, lower power consumption, and increased reliability intensifies. Clock Tree Synthesis (CTS) optimization emerges as a pivotal technique to address these demands. This paper explores the enhancement of VLSI circuit performance through CTS optimization specifically tailored for high-frequency nodes within SoC designs. CTS optimization aims to minimize clock skew, reduce jitter, and ensure precise timing closure, which are critical for maintaining the synchronization of high-speed operations. The integration of advanced CTS techniques, such as Multi-Point Clock Tree Synthesis (MPCTS), plays a crucial role in achieving these objectives. MPCTS leverages multiple clock insertion points, providing a more balanced and efficient clock distribution network that significantly reduces WNS, latency and area.

Keywords: Clock Tree Synthesis, Multi-Point Clock Tree Synthesis, System-On-Chip

1. Introduction

With the continuous increase of clock frequency in chip, the timing closure has become more challenging issue in digital integrated circuit [1-3]. The rapid evolution of semiconductor technology has led to the development of increasingly complex SoC designs, which integrate numerous functional blocks into a single chip. These designs are essential for high performance computing, advanced consumer electronics and cutting-edge communication systems.

CTS is a critical phase in the physical design of VLSI circuits, responsible for distributing the clock signal from the clock source to various sequential elements throughout the chip. In high-frequency nodes, achieving precise timing closure is essential to ensure that all components operate synchronously. Any deviation in clock signal arrival times, known as clock skew, can lead to significant performance degradation, increased power consumption and potential functional failures. Traditional CTS techniques focus on minimizing clock skew and balancing the clock distribution network. However, the increasing complexity and operating frequencies of modern SoCs demand more advanced optimization strategies. This has led to the development and adoption of sophisticated CTS techniques, such as MPCTS, which introduce multiple clock insertion points to enhance clock distribution accuracy and efficiency.

MPCTS offers several advantages over conventional CTS methods, including reduced clock skew, lower jitter, improved signal integrity and enhanced power efficiency. By strategically placing multiple clock points within the design, MPCTS ensures that the clock signal reaches different parts of the chip simultaneously, thus minimizing timing variations and optimizing performance. Effective CTS optimization leads to significant improvements in the overall performance, power consumption, and reliability of the chip. This paper explores the methodologies and strategies employed in CTS optimization, with a focus on enhancing VLSI circuit performance in high-frequency nodes. The findings underscore the necessity of adopting state-of-the-art CTS optimization methods to address the challenges posed by high- frequency operations in VLSI circuits.

The physical design process involves several stages as shown in the Figure1 that transforms a high-level description of a digital circuit into a detailed layout ready for manufacturing. The tool used for implementing physical design process was

Synopsys Fusion Compiler. In Physical design, flow starts with some set of input files and do the sanity check first once the design is loded into PnR tool. In general, there are many iterations are required for a physical design engineer to get a quality floorplan. If a block is macro dominant and cell density is high then the floorplan stage is more critical. The placement phase takes into account the location of power and ground pins and their routing constraints. In Floor Planning step, the overall chip area is divided into logical regions known as blocks. The floor planning process involves deciding dimensions and boundaries of the blocks, the number of components that can be accommodated in each block, and any potential interactions between blocks. There are several placement algorithms available that can optimize for different factors such as power, performance, and area.

Figure 1. Physical Design Flow

The next stage is CTS stage which is mainly concentrated in this paper. CTS is critical in VLSI design, ensuring that the clock signal reaches all parts of the chip simultaneously to maintain synchronization.

Next stage of physical design flow is routing. The goal of the routing process is to interconnect the different components that have been placed on the chip. The routing process involves the creation of networks of wires connecting the various components, ensuring that the connections follow the rules defined by the design. The routing process is computationally intensive and requires the use of specialized algorithms such as maze routing and channel routing to optimize for the best routing solutions.

The next stage is followed by layout Verification. Once the placement and routing are completed, the design layout is verified for compliance with various design rules and specifications. The verification process takes into account the correct placement of components, interconnects, and the overall timing of signals. The design is also checked for any signal integrity issues such as crosstalk and parasitic capacitances.

The final stage is followed by tape-out stage where the design is saved in a format that can be used by the manufacturing process. The output of the physical design process is a set of files that will be used to create photomasks that will imprint the physical design onto the chip during the manufacturing process.

2. Objectives

The objectives of the project is to analyze and reduce the skew and latency in the design using MPCTS. Also by incorporating MPCTS into the design by utilizing drivers with 1-Tap, 3-Tap, and 5-Tap configurations the skew and latency will be met. Also, to evaluate the differences in clock skew and latency among 1-Tap, 3-Tap, and 5-Tap drivers.

3. Methods

High-frequency SoC designs pose unique challenges, requiring advanced CTS optimization techniques to enhance performance, power efficiency, and reliability. This section outlines the strategies for designing and implementing CTS optimization in high-frequency nodes. Some design considerations to be followed in CTS stage can be elaborated as follows

2.1 Clock Tree Architecture

- H-Tree Structure: Utilizes a hierarchical and symmetric tree structure to distribute the clock signal evenly thereby reduces skew.

- Multi Point Clock Tree Synthesis (MPCTS): Introduces multiple clock insertion points to further enhance clock distribution accuracy and minimize skew.

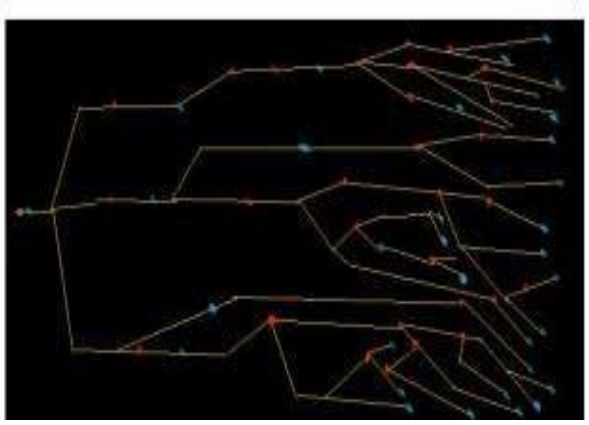
2.2 Buffer Placement and Sizing

Strategic Buffer Insertion: Buffers are placed strategically to drive the clock signal across long distances, reducing skew and improving signal integrity.

- Optimal Buffer Sizing: Select buffer sizes that balance drive strength and power consumption to maintain performance and efficiency.

2.3 Clock Gating

- Local Clock Gating: Implement clock gating at the local level to disable inactive clock branches and reduce dynamic power consumption.
- Global Clock Gating: Apply clock gating at the global level to achieve significant power savings across the entire chip.



- **Figure 2. Stages of Multi Point Clock Mesh**

2.4 Skew Management

- Skew Balancing Techniques: Use zero skew and bounded skew techniques to minimize timing variations.
- Insertion Delay Adjustment: Adjust insertion delays to synchronize clock arrival times across different nodes and reduce overall skew.

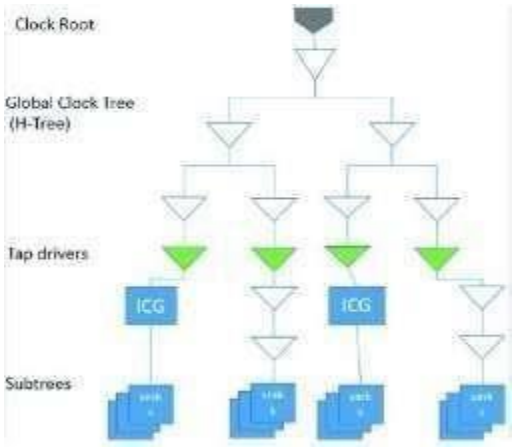


Figure 3. Clock Tree Structure of 3 Tap drivers configuration in CTS

For Implementing clock tree in the design MPCTS is used. The stages for implementing MPCTS is represented in Figure2 as shown above. It involves a global distribution network in form of a sparse mesh or an H-tree with tap points strategically inserted at different locations. These tap points are followed by a local clock tree distribution to route clock from these tap points to the Sequential cell clock end-pins.

MPCTS clock tree structure is shown in Figure 3 which is implemented for 3 tap driver configurations for the design. It consists of the strategic placement of multiple clock insertion points to distribute the clock signal more uniformly across the chip, reducing the distance the signal must travel and thereby minimizing clock skew. This technique also incorporates balancing the clock trees from these multiple points to ensure even distribution and synchronized signal arrival times, which enhances the overall timing accuracy.
Additionally, MPCTS involves the careful placement and sizing of buffers to support the multiple clock paths, maintaining drive strength and minimizing power consumption. Integrating clock gating at both local and global levels is another essential component of MPCTS, reducing dynamic power consumption by disabling inactive clock branches. Verification and analysis, including static and dynamic timing analysis, skew analysis, and signal integrity checks, are crucial to validate the MPCTS implementation, ensuring that the clock network meets stringent timing requirements and performs reliably under various operating conditions.

4 Results

The data furnished below represent the obtained physical design metrics for the implemented MPCTS for different Tap drivers.

Table 1. Timing Analysis for 3 Tap drivers configuration in CTS

Clock	Sinks	Target Skew	Global Skew	Target latency	Max latency	Min latency
CTS	74834	50	217	400	745	528

Table 2. Timing Analysis for 3 Tap drivers in different stages

Clock	Sinks	Target Skew	Global Skew	Target latency	Max latency	Min latency
CTS	74834	50	212	400	652	432

Table 3. Timing Analysis for 5 Tap drivers configuration in CTS

Stage	WNS(Setup) in ps	No of violated paths
Placement	-0.04	3
CTS	-40	230
Routing	-105	311
Route -Opt	-34	22
Re Route	-25	16

Stage	WNS(Setup) in ps	No of violated paths
Placement	-6.8	15
CTS	-70	691
Routing	-108	2670
Route -Opt	-62	718
Re Route	-39	45

Table 4. Timing Analysis for 5 Tap drivers in different stages

From the above tables we can compare the WNS and no of violated paths in the MPCTS implemented for 3 – tap drivers and 5 – tap drivers. Table 1 and Table 2 overviews the no of sinks present for the implemented MPCTS for 3 – tap drivers and 5 – tap drivers. Also it can be inferred from those tables that Max latency observed in the overall design is less when implemented with 5 – tap drivers compared with the 3 – tap drivers.

By referring to the table2 and table 4 it can be observed that that the no of violated paths are less when implemented with high tap drivers (5 – tap drivers) compared to the less tap drivers (3 – tap drivers). So, its better to use multiple tap drivers for the design to be efficient in terms of Latency, WNS and no. of violated paths.

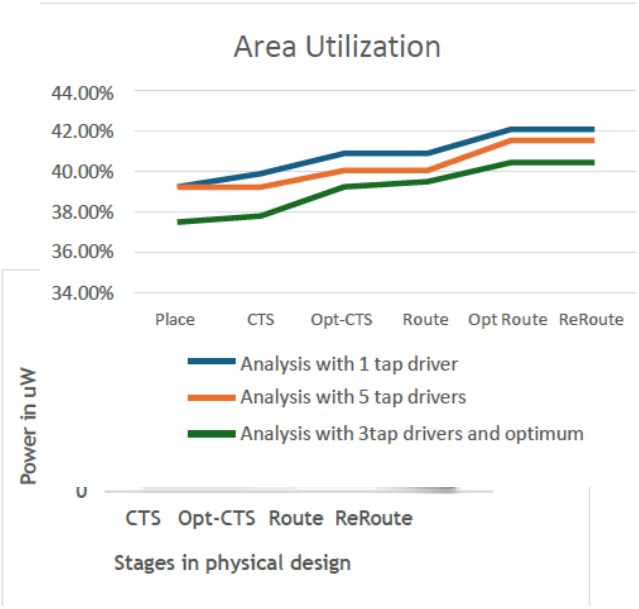


Figure 4. Comparison of area utilization with 1 tap driver, 3 tap driver and 5 tap drivers

The power analysis for 3 – tap drivers and 5 – tap drivers are shown in above figure 4 and figure 5. From this analysis it can be observed that the leakage power in 5 – tap drivers is more compared to that of 3 – tap drivers as many tap points would be present and power requirement would also be more.

The area utilization observed with the different tap drivers is shown in Figure 4. At Re-Route stage it can be observed that the area utilized by 1 tap driver is 42%.and that the area utilized by 5 tap driver is 41.72%, that the area utilized by 3 tap driver with optimum fanout is 40.3%. Hence 5 – tap drivers is good in terms of Area, Latency and WNS.

5 Discussion

Effective CTS optimization is essential for enhancing VLSI circuit performance in high-frequency nodes of SoCs. By leveraging advanced techniques such as Multi-Point Clock Tree Synthesis (MPCTS), strategic buffer placement, and clock gating, designers can achieve superior clock distribution, power efficiency and reliability. This design and implementation guide provides a comprehensive framework for optimizing CTS, driving the development of next generation semiconductor devices.

Addressing the challenges of high-frequency nodes is essential for the successful design and implementation of modern VLSI and SoC architectures. From the above analysis it can be

inferred that using multi – tap points has given several advantages in terms of Timing, area and overall performance of the chip.

References

[1] S. Anirudh and T. K. Ramesh, "An Enhanced Clock Tree Synthesis Methodology for Optimizing Power in Physical Design," *2022 IEEE 3rd International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI SATA)*, Bangalore, India, 2022, pp. 1-9, doi:10.1109/VLSISATA54927.2022.10046629.

[2] A. B. Chong, "Hybrid Multisource Clock Tree Synthesis," *2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, Dubai, United Arab Emirates 2021, pp. 1-6, doi: 10.1109/ICECS53924.2021.9665516.

[3] H. Wang, Q. Lei, Y. Yang, L. Liu and E. Zhao, "A Clock Tree Synthesis Scheme Based On Flexible H-tree," *2022 2nd International Conference on Electrical Engineering and Mechatronics Technology (ICEEMT)*, Hangzhou,China, 2022,pp. 249-252,doi: 10.1109/ICEEMT56362.2022.9862608

[4] E. K. Teh, M. A. M. Zawawi, M. F. P. Mohamed and N. A. Matisa, "Practical full chip clock distribution design with a flexible topology and hybrid metaheuristic technique", *IEEE Access*, vol. 9, pp. 14816- 14835, 2021.

[5] P. Ray, V. S. Prashant and B. P. Rao, "Machine Learning Based Parameter Tuning for Performance and Power optimization of Multisource Clock Tree Synthesis," *2022 IEEE 35th International System-on-Chip Conference (SOCC)*, Belfast, United Kingdom, 2022,
pp. 1-2, doi: 10.1109/SOCC56010.2022.9908123.

[6] L. S. P, S. R. R. A, V. Pudi and N. T. B. M, "A Configurable Multi Source Clock Tree Synthesis For High Frequency Network On Chips," *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, Monterey, CA, USA, 2023, pp. 1-5, doi: 10.1109/ISCAS46773.2023.10181875.

[7] N. Uysal and R. Ewetz, "An OCV-Aware Clock Tree Synthesis Methodology," *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Munich, Germany, 2021, pp. 1- 9, doi: 10.1109/ICCAD51958.2021.9643585.

[8] V. G. Srivatsa, A. P. Chavan and D. Mourya, "Design of Low power & High Performance Multi Source H-Tree Clock Distribution Network," *2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS)*, Kolkata, India, 2020, pp.468-473,doi: 10.1109/VLSIDCS47293.2020.9179954.

[9] M. Choi, D. Oh and J. Kim, "Slew-aware fast clock tree synthesis with buffer sizing," *2018 International Conference on Electronics, Information, and Communication (ICEIC)*, Honolulu, HI, USA, 2018, pp. 1-4, doi: 10.23919/ELINFOCOM.2018.8330581.

[10] D. K. G, R. Srinidhi and S. P, "Physical Implementation of Low-Power Area- efficient Digital Delay Locked Loop for High-Speed Interface in Sub -10nm Technology," 2022 International Conference on Computing, Electronics & Communications Engineering (iCCECE), Southend, United Kingdom, 2022, pp. 21-24, doi: 10.1109/iCCECE55162.2022.9875101.

Augue interdum velit euismod in pellentesque massa placerat duis ultricies. Metus aliquam eleifend mi in nulla posuere sollicitudin aliquam ultrices.

Velit laoreet id donec ultrices tincidunt arcu non sodales neque. Non curabitur gravida arcu ac tortor dignissim convallis aenean et.