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Design and Characterization of a 4:1 standardMGDI Mux cell

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***Abstract*—This study investigates the design and characterization of a 4:1 multiplexer (MUX) with high efficiency and low power [2] that is achieved by using of an Enhanced Modified Gate Diffusion Input (MGDI) technique. When compared to conventional CMOS designs, the MGDI approach dramatically lowers the number of transistors needed, increasing operational speed and power efficiency. We suggest an enhanced MGDI technique in order to solve the problem of swing degradation present in the original MGDI method. The performance of the proposed 4:1 MUX was assessed through simulations conducted in Cadence Virtuoso, revealing a substantial reduction in both dynamic and static power consumption as well as minimized propagation delay.The simulation outcomes indicate that the enhanced MGDI-baseddesign offers superior performance, making it ideal for high-speed, low-power applications in contemporary VLSI systems.**

***Index Terms*—GDI, Modified GDI, Full Swing, Low Power Consumption,Multiplexer**

INTRODUCTION AND OPTIMIZATION TECHNIQUE

In digital integrated circuits, the multiplexer (MUX) is a fundamental component that is used to select one of several input signals and transfer the selected input to a output line. The efficiency and performance of a MUX significantly impact the overall functionality and power consumption of digital systems, particularly in complex VLSI designs. The goal isto achieve high performance and low power consumption [9]. The paper covers the design methodology, simulationresults, and performance metrics such as power efficiency and propagation delay, demonstrating the advantages of the MGDI approach over conventional CMOS designs in the context of VLSI systems.

A. GDI Technique Basics

Two transistors, NMOS and PMOS, make up the basic GDIcell. Each transistor has four terminals: G is the common gate input, P is the PMOS outer diffusion node, N is the NMOS outer diffusion node, and D is the common diffusion node. A multiplexer function utilizing the fundamental GDI cell is shown in Figure 1.

The drawbacks of the GDI technique includes, Inadequate biasing of the bulk terminals causes threshold drops and Vt fluctuations in the circuit. Furthermore, floating bulk terminals result in greater static power dissipation and higher fabrication costs. One major drawback is that whether the PMOS transmitsa logic 0 or the NMOS transmits a logic 1, the output deteriorates.

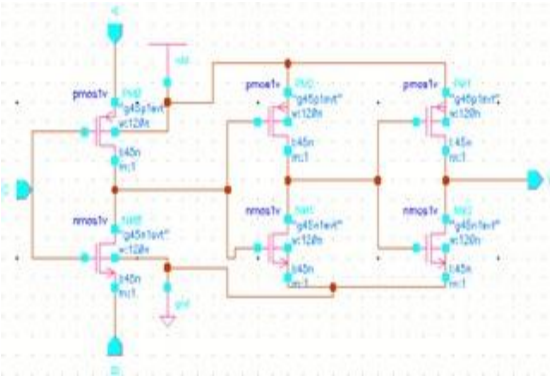

Fig. 1. 2:1 Mux using MGDI technique

B. Improved MGDI technique.

As shown in Figure 2, the substrate terminals of P bulk and N bulk transistor in this technique directly connected to VDD and GND respectively. This configuration enhances delay and lessens output swing degradation. The benefits of the

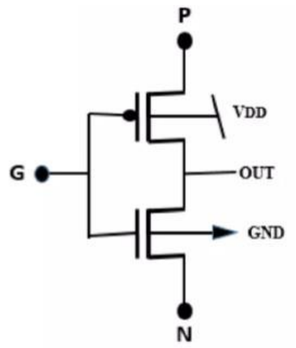

Fig. 2. Basic connection in MGDI technique

enhanced MGDI method are discussed in this section [8]. It is suitable for the CMOS n-well and p-well procedures of logic cell fabrication and efficiently handles threshold drop changes. This arrangement improves logic swing by including more transistors, such as NMOS for stronger logic 0 and PMOS for stronger logic 1. The schematic implementation of 2 :1 mux is shown in Figure 3.

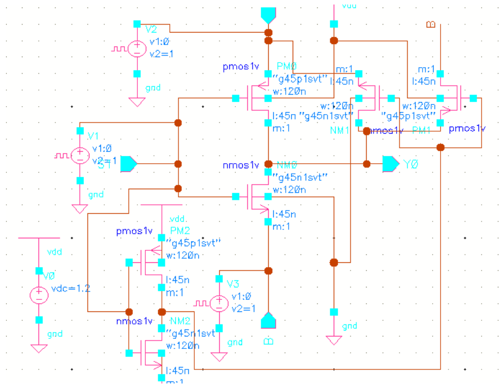

Fig. 3. 2:1 Mux using improved MGDI technique

I. Methodology

The choice of cells or logic gates for building a library depends on the specific design requirements. In a Semi- Custom Design Flow, these cells must fulfill certain functional and performance criteria. Cells can be optimized for either area or speed, area-optimized cells use the smallest possible transistors, while speed-optimized cells use larger transistors to enhance driving capabilities.

phase, a transistor-level schematic of the cell is created using design tools, ensuring it meets the initial specifications.

After completing the schematic, a symbol representing it is created for integration into higher-level circuit designs. Pre- layout simulations are performed on the schematic to verify its functionality and performance, allowing designers to detect and correct any issues before moving forward. The subsequent step is the layout phase, where the physical arrangement of the standard cell is created, including the placement and routing of transistors and their interconnections. This layout must adhere to the design rules of the technology being employed [6].

Characterizing a 4:1 multiplexer (MUX) involves assessing its performance based on critical metrics such as power con- sumption, delay, and area efficiency. A 4:1 MUX selects one of four input signals based on two selection lines and outputs the chosen signal. In contemporary VLSI design, achieving high performance and low power consumption is essential. This method reduces transistor count, dynamic power consumption, and propagation delay as compared to traditional CMOS designs.

This design is implemented using 45nm technology, bal- ancing performance, power, and cost. It operates at a supply voltage of 0.9V to 1.0V for low-power efficiency. A 2:1 PMOS to NMOS ratio is adopted for balanced performance, minimizing delay and power. Load capacitance is minimized to reduce dynamic power and delay. The design is optimized for operation across a wide temperature range (0°C to 100°C) and is validated across various process corners (TT, FF, SS, FS, SF) to ensure robustness against manufacturing variations.

The dynamic power calculation is shown below

$$P_{dyn} = \alpha \times C_L \times V_{DD}^2 \times f \quad (1)$$

$$C_L = \frac{P_{dyn}}{\alpha \times V_{DD}^2 \times f} \quad (2)$$

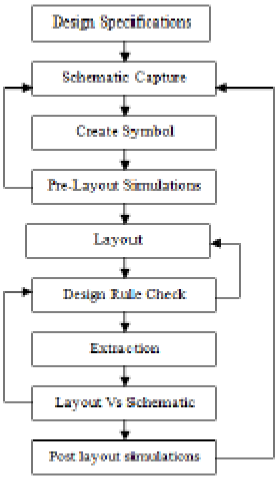

Fig. 4. Design flow for standard cell

The development of each cell in the library follows a Bottom-Up design approach, as depicted in Figure 4 [2]. The standard cell design process is a systematic method used to design, verify, and characterize integrated circuits (ICs). It starts with defining the design specifications, which encom- pass the functional requirements, performance objectives, and constraints for the standard cell. Next, in the schematic capture600

10^{-3} W

C_L = $0.5 \times (1.2\ \text{V})^2 \times 2 \times 10^9$ Hz

$C_L \approx 208$ pF

A 4:1 multiplexer (MUX) can be efficiently constructed using three 2:1 MUX by arranging them in two stages [1].To design 2:1 we require total of 6 transistors as shown in fig

2. By Using these 2:1 mux structure we are constructing 4:1 mux which is in 2 stages. For 4:1 mux overall it required 14 transistors as shown in figure 4.

The delay of a 4:1 MUX can be approximated by the sum of the delays through each logic gate in the critical path.In power Consumption Calculation There are two types of Powerconsumption present In circuit that are Dynamic power and static power [7].Here we have calculated dynamic power as follow.

All the Standard cells are in equal in height and varying width [3]. Main characteristics of a standard cell have been explained

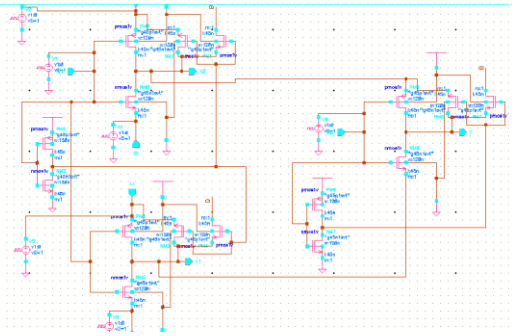

Fig. 5. 4:1 mux using improved MGDI

with the help of the following figure 4.1. At the top of the standard cell, there is VDD rail and bottom there is a VSS rail. Both the Power rails are drawn in the Metal-1 layer.

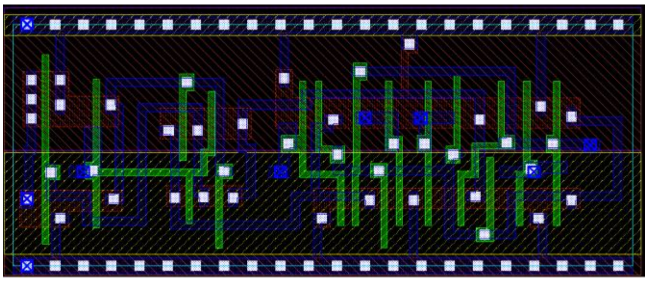

Fig. 6. Layout diagram of 4:1 standard cell

(3)

×

(4)

II. Characterization

Evaluating a 4:1 multiplexer (MUX) designed with Modi- fied Gate Diffusion Input (MGDI) logic requires analyzing its power consumption and delay characteristics. By employing Monte Carlo simulations [5], we can consider process varia- tions and confirm reliable performance under various manu- facturing conditions and temperatures. This section details the methodology and findings of the power and delay analysis of the MGDI-based 4:1 MUX cell, incorporating rise time, fall time, and Monte Carlo simulations [8].

A. Monte Carlo simulation

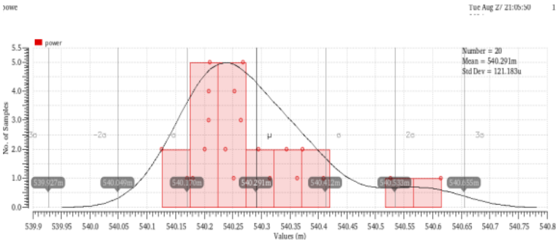

Fig. 7. Monte Carlo simulation for Power variation

The power characterization includes calculation of total power under various operating conditions. Dynamic power is consumed when the MUX switches states [3]. It includesTable Ipower Variations Wrt Temperature

	Mim(mW)	Max(mW)	Mean(mW)	StdDev(mW)
Power	591	603.9	597.7	2.217
Power Best	591.2	601.9	597.2	2.217
Power regular	591	601.9	597	2.217
Power worst	594.5	603.6	599.7	1.8

capacitive charging and discharging of internal nodes.

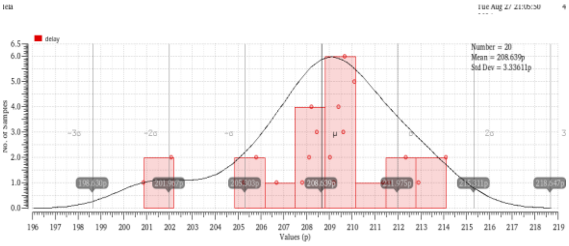

Fig. 8. Monte Carlo simulation for dalay variation

The delay characteristics are to calculate the delay delay using the rise time and fall time [9]. Propagation time is the time it takes for an input change to propagate through the MUX to cause a proportional change to the output. The average of the rise and fall propagation delays. It represents the overall delay of the signal through the MUX.

Table Ii Delay Variations Wrt Temperature

	Mim(ps)	Max(ps)	Mean(ps)	StdDev(ps)
Delay	66	102.6	81.2	6.056
Delay Best	50.78	77.94	61.76	4.761
Delay regular	66.64	102.6	81.2	6.0563333
Delay worst	65.88	101.4	80.27	5.998

B. *Corner Analysis*

Corner analysis was performed to evaluate the performance of the 4:1 MGDI multiplexer across different process, volt- age, and temperature (PVT) corners. The corners considered include:SS (Slow-Slow), TT (Typical-Typical), FF (Fast-Fast), SF (Slow-Fast), FS (Fast-Slow).

Table Iii Corner Analysis Of Voltage And Delay With Respect To Ff Corner

	CO 0	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	CO 7	CO 8
Voltage(V)	1.1	1.1	1.1	1.2	1.2	1.2	1.3	1.3	1.3
Corner	ff	ff	ff	ff	ff	ff	ff	ff	ff
Temperature(°C)	0	27	99	0	27	99	0	27	99
Power(mW)	662.8	662.7	662.4	722.5	722.4	722.1	782.1	782.0	781.6
Rising(ps)	11.18	12.8	17.52	11.34	12.81	17.74	12.28	14.63	19
Falling(ps)	9.845	10.99	14.8	7.933	8.815	11.74	6.758	7.461	9.627
Delay(ps)	88.01	93.83	110.9	89.58	95.5	112.8	92.39	98.51	116.1

Table Iv Corner Analysis Of Voltage And Delay With Respect To Fscorner

	CO 0	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	CO 7	CO 8
Voltage(V)	1.1	1.1	1.1	1.2	1.2	1.2	1.3	1.3	1.3
Corner	fs	fs	fs	fs	fs	fs	fs	fs	fs
Temperature(°C)	0	27	99	0	27	99	0	27	99
Power(mW)	663	652.9	662.6	722.6	722.5	722.2	782.3	782.1	781.7
Rising(ps)	11.08	12.39	17.21	10.43	11.85	17.57	10.06	11.58	15.57
Falling(ps)	11.04	12.32	16.85	8.547	9.791	12.87	7.779	8.017	10.23
Delay(ps)	99.97	106.5	125.4	101.1	107.8	126.8	102.9	109.8	128.9

Here in table 5.3 the fast-slow (FS) corner presents a mixed scenario where the PMOS transistors are fast, leading to quick rising edges, but the NMOS transistors are slow, resulting in slower falling edges. This asymmetry in transistor performance can affect the overall timing balance of the circuit.

Table V Corner Analysis Of Voltage And Delay With Respect To Sfcorner

	CO 0	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	CO 7	CO 8
Voltage(V)	1.1	1.1	1.1	1.2	1.2	1.2	1.3	1.3	1.3
Corner	sf	sf	sf	sf	sf	sf	sf	sf	sf
Temperature(°C)	0	27	99	0	27	99	0	27	99
Power(mW)	661.8	661.7	661.3	721.4	721.3	720.9	781.1	780.9	780.4
Rising(ps)	14.07	16.29	23.3	15.82	18.02	25.51	18.08	20.32	27.8
Falling(ps)	10.66	12.03	15.77	8.513	9.592	12.83	7.223	8.042	10.34
Delay(ps)	123.7	131.1	152.4	124.1	131.4	152.2	124	131.1	151.9

Here in table 5.4 the slow-fast (SF) corner presents a scenario where the PMOS transistors are slow, leading to increased rising delays, while the NMOS transistors are fast, maintaining the falling delays at levels comparable to the best-case FF corner. This asymmetry in transistor performance can create challenges for circuit designers, particularly in applications where balanced rising and falling delays are important. SS Configuration Offers the worst performance due to both transistors being slow. SF Configuration Offers intermediate performance with fast NMOS and slow PMOS.

Table Vicorner Analysis Of Voltage And Delay With Respect To Ss Corner

	CO 0	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6	CO 7	CO 8
Voltage(V)	1.1	1.1	1.1	1.2	1.2	1.2	1.3	1.3	1.3
Corner	ss	ss	ss	ss	ss	ss	ss	ss	ss
Temperature(°C)	0	27	99	0	27	99	0	27	99
Power(mW)	661.8	661.6	661.3	721.3	721.1	720.6	780.8	780.6	779.9
Rising(ps)	14.46	15.67	23.17	14.82	16.62	23.18	14.78	16.66	24
Falling(ps)	11.91	15.32	17.98	13.91	13.3	18.13	7.613	8.422	10.634
Delay(ps)	142.4	151.1	176.6	143.6	152.2	177.7	144.7	153.3	178.9

The results from the functional verification, Monte Carlo simulations, and corner analysis provide a comprehensive understanding of the performance of the 4:1 MGDI Mux cell.The design meets the functional requirements and exhibits good robustness against process variations and PVT corners.

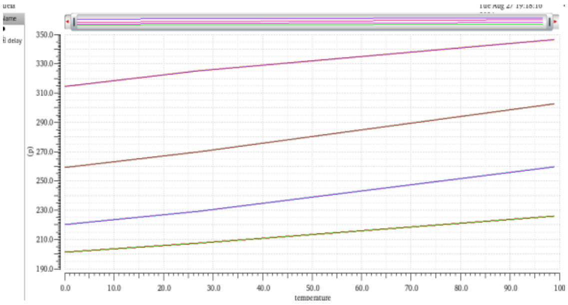

Fig. 9. PVT variation of delay wrt temperature

The FF corner typically exhibits the fastest performance, while the SS corner is the slowest. FS and SF can present unique challenges due to transistor mismatch, potentially caus- ing timing violations. The variation of mux delay with respect to voltage and temperature is shown in above graph.

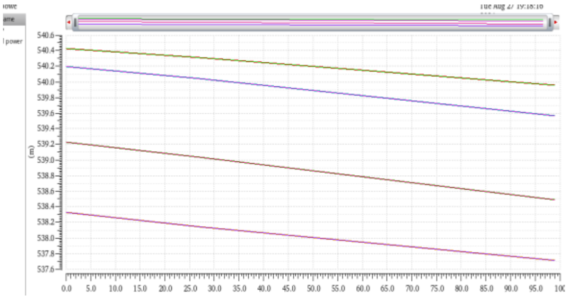

Fig. 10. PVT variation of power wrt temperature

FF tends to consume the most power, while SS is the most power-efficient. FS and SF consume intermediate levels of power, but this can be design-dependent.The variation of mux power with respect to voltage and temperature is shown in above graph.

III. Results

By analysing the results obtained from simulation its clearer that the improved MGDI method performs better interms of delay and power consumption. And also improved MGDI technique requires less number of transistors.The results are tabulated in table-3 The Figure 7 shows the Bar graph for the comparison of delay and power. it implies that the improve- ment in power is less compared to improvement in power.

TABLE VII COMPARISON TABLE OF SIMULATION RESULT

	MGDI	improved MGDI
Power	567.9 mW	523.3 mW
Delay Best	1.37 ns	81.2 ps
an Count	16	14

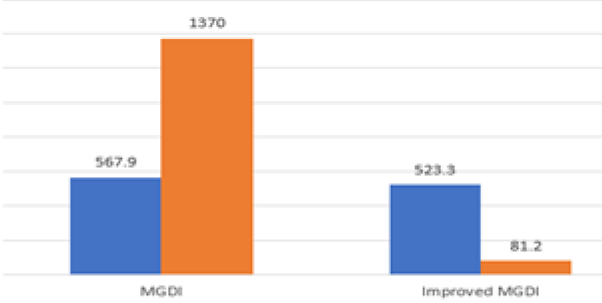

Fig. 11. Graph shows comparison of different mux result

IV. Conclusion

The study details the design and characterization of a 4:1 multiplexer using the (MGDI) technique. It outlines the theoretical fundamentals, design specifications, and implementation strategies, followed by simulation and performance evaluation. The MGDI technique's advantages are highlighted through detailed results, including functional verification and Monte Carlo simulations.The design of Mux is carried out in cadence virtuoso.The characterization with Monte Carlo simulation is performed in cadence Liberate tool. The results quantifies that the Improved MGDI offers 41% improvement in the delay and 12% improvement in the power efficiency

.Also results demonstrates that the Improved MGDI offers significant advantages over the original MGDI, including enhanced energy efficiency, reduced delay, and optimized transistor count.

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