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Boosting FIR Filter Performance: A Novel Approach Using Approximate Kogge-Stone Adders and Vedic Multipliers

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Abstract

The efficiency of multipliers is crucial in digital signal processing. Vedic multiplication algorithms offer exceptional speed and performance advantages. This study compares the area, power, and timing attributes of different models and shows optimized performance in the proposed model. The parameters of power, area, and timing improved by 31.94%, 30.59%, and 1.03%, respectively, when comparing adders. Conversely, when compared with filters, these parameters show a more modest enhancement of 8.72%, 6.9%, and 0.76%, respectively. This realistic comparison underscores the practicality of our research findings.

Keywords: Parallel prefix adder, Vedic multiplier, FIR filter, Kogge-stone, power utilization, optimization

1. Introduction

Approximate computing (AxC) is a new design paradigm aimed at increasing efficiency across the computing stack by taking advantage of the fault resilience of many applications [1, 2]. AxC introduces accuracy as a new dimension for trade-offs in design optimizations, significantly reducing VLSI circuit area and energy consumption for computations [3] [4, 5]. Many complex applications require numerous adder units in hardware accelerators. These adder units are essential building blocks and can be used with other approximate arithmetic units for various approximations [6, 7]. Multiple studies have proposed architectures for Approximate Adders (AxAs). The energy-efficient AxAs replicate the logic of the lower part of the adder from the least significant bits (LSBs) to the most significant bits (MSBs) [8-10]. Among the fastest and most area-efficient addition units are the Parallel Prefix Adders (PPAs), which utilize logarithmic reduction of carry propagation paths to optimize the delay of critical paths [11-13]. Optimizing the circuit synthesis of PPAs represents a significant challenge in digital hardware design. This article introduces Approximate PPAs (AxPPAs) that combine logical approximations from LSB to MSB and fast carry propagation, offering a hybrid solution for both fast and energy-efficient adders [14, 15]. Our approach not only demonstrates a new AxA Pareto front of circuit area and energy reduction for the same level of approximation, but also promises significant benefits in terms of area, time delay, and energy efficiency.

The research is centred on approximating the logic of carry propagation (P) and generation (G) of prefix operators (POs). This involves the implementation and evaluation of four AxPPAs using Brent Kung (AxPPA-BK), Kogge Stone (AxPPA-KS), Ladner-Fischer (AxPPA-LF), and Sklansky (AxPPA-SK) architectures [16, 17] [18] [19] [20]. To substantiate their applicability, we apply these proposed AxPPAs in various contexts, such as finite impulse response (FIR) filters and the sum of squared differences (SSDs) pixel comparisons for block matching in video processing [21-23]. FIR filters and SSD applications serve as relevant case studies due to their utilization of numerous adders, impacting area, delay, and power dissipation. Notably, the FIR filter employs adders to accumulate the generation of the inner product of vector-to-vector multiplication in the convolution step [24]. Conversely, the SSD hardware architecture comprises a summation tree for aggregating partial values. Furthermore, the addition tree in both case studies facilitates the exploration of efficient addition schemes, including the combinations of AxA.

The article is structured as follows: Section 2 provides an overview of related works. Section 3 presents an overview of approximate PPAs. Section 4 delineates our objective and proposed work, and Section 5 presents the results of the RTL view and

their corresponding output waveforms from Xilinx. Finally, Section 6 summarizes the principal findings and compares the contribution of the work.

2. Related works

The emergence of approximate arithmetic units has garnered substantial research attention, primarily driven by their potential to economize circuit area, minimize time delays, and conserve energy. Several scholars have introduced AxA architectures, which are designed to enhance the performance and efficiency of digital circuits. In these architectures, the primary focus is on either reducing latency or critical path by shortening the carry-propagation chain or minimizing power consumption by eliminating carry calculations and other circuit logic. In our work we compare the parameters area, power and time delay with existing and proposed model. The paper [25] introduces a high-speed multiplier using Vedic Maths and a half-adder in VHDL, which is more efficient in terms of area and speed compared to other multiplier architectures. Similarly [26], proposed a modified binary Vedic multiplier using ancient Vedic mathematics, incorporating improvements in time delay and device utilization. The technique was designed using Kogge Stone adder and implemented in Verilog HDL, with simulations conducted for 4-bit, 8-bit, 16-bit, and 32-bit multiplication operations. Results are shown only for the 32-bit binary Vedic multiplier, with potential for extension to larger sizes. The advancement of CMOS technology requires redesigning functional digital system units, such as the 64-bit parallel-prefix adder presented in this paper [27]. It consumes significantly less energy compared to other designs in various technology nodes. In contrast, The FIR Filter has various applications in signal processing, biomedical applications, and de-noising. In the work [28], they designed the FIR filter using parallel prefix adders and compared its performance with the conventional ripple carry adder-based FIR filter. The simulation was conducted using Xilinx version 14.2. Quality evaluation metrics such as power, area, and delay were measured using Cadence 180nm technology. The proposed design outperformed the conventional design in terms of power, area, and delay.

Identically [29] introduces a unique approximate adder that improves computing accuracy and hardware efficiency through error-reduced carry prediction and constant reduction techniques. Compared to other approximate adders, the proposed carry forecast technique lowers prediction error rates. The adder's error reduction technique enhances overall computation efficiency by reducing the error distance (ED). It makes it cost-effective, with minimal impact on quality attributes in application areas such as digital image processing and machine learning. Likewise [30] discusses the ancient Vedic mathematics, which includes 16 sutras and 13 subsutras for arithmetic calculations. The paper presents a 32-bit Vedic multiplier using the Urdhva Tiryagbhyam sutra. This multiplier is designed using 16-bit multipliers and adders, providing fast computation with minimal time delay and fewer slice LUTs. The paper also covers the methodology of implementation and discusses the delay and number of slice LUTs for the implemented 32-bit multiplier. Comparatively [19] explored Reconfigurable FIR filters are commonly used in wireless communications and digital signal processing. We are proposing a modified FIR filter design to reduce power, time, and area compared to traditional designs. This modification involves replacing the Wallace adder with a carry-select adder, resulting in lower delay, power, and area consumption. The study by [31] aims to enhance the efficiency of DSP systems by designing circuits that approximate calculations. A proposed RoBA multiplier type rounds numbers to the closest whole number, simplifying the multiplication process and reducing system size. Comparing the Vedic and ROBA multipliers showed significant reductions in power, area, and delay while increasing the multiplier speed. In contrast [32] focuses on optimizing a finite impulse response (FIR) filter for VLSI implementation to reduce power consumption and hardware complexity. It explores different multiplication techniques and concludes that the best-optimized filter is the FIR filter using the Wallace tree (WT) multiplier. In comparable, [33] desires to enhance filter design for optimal circuit design. It focuses on improving the performance of VLSI circuits in areas of power and delay. The goal is to reduce the number of adders and multipliers using various computational

algorithms. The proposed method utilizes enhanced Vedic multiplication logic and improved carry-look ahead adder logic. Power optimization is achieved using an enhanced clock gating technique. The design is compared with conventional FIR filter designs, showing improvement in area, power, and delay. In Contrast, [34] explored a new FIR filter has been designed using the Enhanced Squirrel Search Algorithm (ESSA) and Variable Latency Carry Skip Adder (VL-CSKA) based booth multiplier. The ESSA algorithm selects an optimal FC, while the VL-CSKA-based booth multiplier reduces the delay of the FIR filter with the parallel addition of partial products (PPs). The proposed FIR filter outperforms the state-of-the-art FIR filters by consuming only 0.142 mW power with a delay of 28.175 ns, according to simulation results. In the paper [35], they propose an approximate multiplier circuit with two different architectures for digital signal processing applications. Two methods were used to implement approximate multipliers for image processing using Xilinx ISE 14.7 and Verilog HDL coding. Based on our current understanding, the literature outlines various approaches to optimizing PPAs and Vedic multipliers in the realm of DSP applications. Of particular note is the introduction of AxPPAs, which serve as a comparative tool for area, power, and time delay evaluations. This methodology aligns with the specific approach we have developed in our work.

3. Approximate Parallel Prefix Adder

Approximate parallel prefix adders offer a balanced approach to designing arithmetic circuits, focusing on computational precision, efficiency, and resource utilization [36-38]. In traditional digital systems, parallel prefix adders are commonly employed for rapid and efficient addition operations [39]. However, the attainment of high precision in these systems often entails heightened hardware intricacy and power consumption. In contrast, approximate parallel prefix adders deviate from the conventional paradigm by giving priority to speed and resource efficiency over absolute precision [40]. These adders leverage approximation techniques to compromise a certain degree of accuracy for improvements in speed, area, or power consumption [29]. By relaxing the necessity for perfect accuracy, approximate parallel prefix adders offer a promising avenue for optimizing the performance of arithmetic circuits across various applications, encompassing digital signal processing, image processing, and machine learning [41]. The design of approximate parallel prefix adders involves integrating approximation algorithms, error estimation mechanisms, and optimization methods to attain a balance between precision and constraints [27]. Designers can use various approximation strategies to customize adder performance. Approximate adders offer performance improvements without compromising system functionality and enable trade-offs between accuracy, speed, and energy efficiency for specific use cases or deployment scenarios [42] [18]. Combining approximate parallel prefix adders and Vedic multipliers optimizes FIR filter performance, power consumption, and resource utilization [43]. The paradigm uses FIR filters for improved speed and resource usage, while Vedic multipliers reduce delay and area overhead [44] [45]. Through the exploitation of parallel computation and effective hardware implementation, Vedic multipliers elevated the multiplication operations within FIR filters, resulting in amplified throughput and decreased latency [46]. The integration of approximate parallel prefix adders and Vedic multipliers enhances FIR filter implementations for diverse signal processing applications, reducing hardware complexity and resource utilization [47].

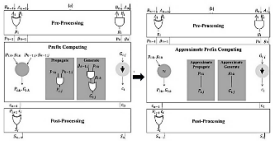

Fig.1. Approximate parallel prefix adder

4. Objectives

- To design and implement the 16-bit Kogge stone adder and 8x8 Vedic multiplier
- To design FIR Filter with Approximate Kogge stone adder and Vedic Multiplier
- To investigate area, power and Time delay for the base and proposed model
- To compare power utilization, area and time for existing and proposed techniques and to optimize the result of the proposed structure

5. Proposed work

The Brent-Kung adder, Sklansky adder, Ladner-Fischer adder, and Kogge-Stone adder are all examples of parallel prefix adders, which are used in digital circuit design to perform fast arithmetic operations. In the specific context of our project, we have chosen to utilize the Kogge-Stone adder for its efficient parallel computation capabilities. Furthermore, in addition to implementing the Kogge-Stone adder for the addition process, we are concurrently engaged in the development of a finite impulse response (FIR) filter. This involves the utilization of both an approximate Kogge-Stone adder and a Vedic multiplier, aiming to achieve higher throughput and performance in our digital signal processing application. This research is specifically focused on developing an optimized FIR filter to be used in DSP applications. The filter is designed to seamlessly integrate Parallel prefix adder (PPA) and Vedic multiplier, with the primary goal of enhancing power efficiency, minimizing time delay, and maximizing area efficiency. Through the utilization of Verilog HDL and Xilinx 14.7 ISE tools, significant enhancements have been achieved in both power and area efficiency, as well as notable reductions in delays.

a) Proposed approximate parallel prefix Kogge-stone adder

The proposed model aims to streamline hardware complexity and reduce power consumption by implementing reduced-precision arithmetic and simplified logic gates. This approach is anticipated to significantly enhance overall performance. Comprehensive simulation and synthesis experiments will be conducted to thoroughly assess the model's effectiveness in terms of power consumption, delay, and accuracy. The visual representation of the proposed design is presented below for your reference.

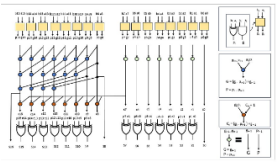

Fig.2. Proposed AxPPAs Kogge stone adder

6. Results

6.1 Design of 8x8 Vedic Multiplier

During the initial phase of development, the Vedic Multiplier was initially designed employing a 2x2-bit multiplier. Subsequent iterations saw a significant evolution in the design, expanding this configuration to accommodate a 4x4 Vedic multiplier, which effectively served the purpose of synthesis. To enhance the accessibility of the specific architecture, a meticulously engineered Ripple carry adder was integrated within the 4x4 Vedic Multiplier. The final stage of the implementation process of the 8x8 Vedic multiplier involved its integration with the 4x4 Vedic Multiplier, culminating in the creation of a comprehensive multiplication system. In conjunction with this phase, an 8-bit ripple carry adder was diligently devised to facilitate the precise operation and coordination of the 8x8 multiplier. The detailed schematic of this addition can be observed in Figure 20, offering a visual representation of its integral role within the overall system.

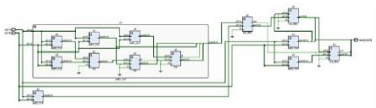

Fig.3. 8x8 Vedic Multiplier in Xilinx

After performing meticulous and extensive testing utilizing a comprehensive test bench, we have validated that the design functions accurately and reliably across a diverse array of conditions. These conditions encompass variations in Functionality and other factors. Through a rigorous and comprehensive testing process, we guarantee that the design operates reliably and consistently in a diverse array of real-world situations, as depicted in Figure 4.

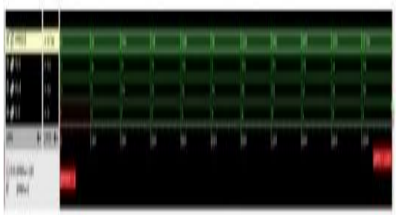

Fig.4. Simulation result of 8x8 Vedic multiplier in cadence

6.2 Design of FIR Filter with Kogge Stone Adder and Vedic Multiplier

The Finite Impulse Response (FIR) filter, a fundamental component in digital signal processing, can be implemented using the previously developed Kogge Stone adder and Vedic Multiplier. The process follows the specific principles outlined in Figure 2, incorporating the

principles of digital filter design to achieve the desired filtering characteristics. When incorporating this filter, it is vital to align its timing with the system clock meticulously. This ensures that the filter operates with precision and consistency, seamlessly integrating into the system to deliver optimal performance. This precise synchronization is essential for maintaining accurate timing and enhancing overall system efficiency. Careful incorporation of the reset mechanism is essential to guarantee proper initialization and operation under all conditions. Ensuring a seamless integration of the D flip-flop is crucial for preserving the integrity and efficiency of the filter within the current system. This integration is necessary to maintain the overall functionality and performance of the system.

6.3 Design of FIR Filter with Approximate Kogge Stone Adder and Vedic Multiplier

Our proposed design model has been effectively implemented through the integration of both the approximate Kogge Stone adder, known for its high-speed parallel computation capabilities and the Vedic multiplier, a technique derived from ancient Indian mathematics that is adept at performing fast arithmetic operations. This integrated approach has led to significant improvements in our design's computational efficiency and performance. This groundbreaking approach represents a major milestone in our research endeavours, showcasing the successful integration of cutting-edge computational methods aimed at significantly enhancing the overall performance and efficiency of our system. Figures 8 and 9 provide a visual representation of the simulation of the approximate Finite Impulse Response (FIR) filter conducted in Cadence, a significant electronic design automation software. In addition, these figures depict the results of the real value simulation of the newly proposed FIR filter. This demonstrates the performance and behaviour of the filter in a visual format, allowing for a comprehensive understanding of its operation and effectiveness. These simulations serve as a testament to the efficacy and potential impact of our innovative methodologies.

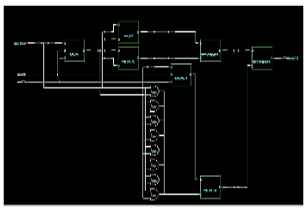

Fig.5. RTL Schematic of Approximate FIR Filter in cadence

Fig.7. Real value simulation results of proposed FIR Filter

7. Comparative Analysis of both Models

The table 1 presented below outlines the comprehensive details of every parameter for both our base model and the proposed model. This includes a breakdown of all variables, specifications, and configurations essentials for each model.

Table.1. Data for Area, Power and Timing for Base model and proposed model

Parameter	Kogge Stone	8x8 Vedic Multiplier	Base FIR filter	Approximate Kogge Stone	Proposed FIR Filter
Power	5.51E-06	2.18E-05	6.65E-04	3.75E-06	6.07E-04
Area	265.05	574.218	2347.824	183.996	2185.722
Timing	1.94E-10	9.23E-10	1.31E-09	1.92E-10	1.30E-09

In the thorough examination, we performed a detailed comparative analysis to contrast the operational performance of the conventional Kogge stone adder with an advanced version. Our study encompassed an extensive comparison between the basic FIR base filter, which serves as a foundation, and an elaborately enhanced FIR filter proposal. The comparison delved into their respective filtering mechanisms, scrutinizing their ability to process and manipulate signals effectively. Additionally, the analysis examined

their computational efficiencies, including factors such as processing speed, power utilization, and overall performance in real-world applications.

Table.2. Comparison for Area, Power and Timing for Base model and proposed model

Parameters	Comparison b/w adders	Comparison b/w Filters
Power	31.94%	8.72%
Area	30.59%	6.9%
Timing	1.03%	0.76%

8. Conclusion

In digital signal processing, the efficiency of multipliers is crucial due to their impact on circuit complexity. Vedic multiplication algorithms are renowned for their speed and performance. Our research combines approximate parallel prefix adders and a Vedic multiplier with an FIR filter to handle partial products. After rigorous testing and analysis, we have achieved optimized results in area, power utilization, and time delay. When comparing adders, the parameters of power, area, and timing improved by 31.94%, 30.59%, and 1.03%, respectively. Conversely, when compared with filters, these parameters show a more modest enhancement of 8.72%, 6.9%, and 0.76%, respectively. After calculating all the parameters, we can observe a 0.57% tradeoff for overall efficiency. Comparisons have demonstrated significant improvements in performance metrics. This applies the groundwork for future research to enhance these results further.

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