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Design and Analysis of Phase Locked Loop for SPI and I2C protocols

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Abstract - Phase locked loops (PLL) is mainly used in Communication-Systems, Micro-Processor, Networking , as well as Frequency-Synthesizers which are used in Clock-Generation along with Clock-Recovery. PLL(Phase-locked loops) being extensively utilized in digital systems which require higher performance for generating On chip clocks which have been well timed. Our Current Wireless systems of communications utilize PLL(Phase-Locked Loop) primarily to reduce Synchronization , the Clock-Synthesis, as well as skewing and jitter. Due to circuit operations increased speed, a faster locking capability circuit of PLL is needed. Here different blocks of PLL such as Phase detector, Charge Pump, Low Pass Filter and VCO are designed and focused to attain frequency of 3.5MHz for high speed mode of I2C protocol and default operating frequency of 1MHz for SPI protocol. Developing a Layout for the final design. The PLL blocks are implemented in CADENCE Virtuoso(90-nm) technology.

Keywords— Phase detector, Charge Pump, Low Pass Filter, VCO, SPI Protocol and I2C Protocol

1. Introduction

Elevated products such as televisions and cell phones are in more demand due to the development of portable electronics brought about by the introduction of contemporary electronics. These mobile devices need to have circuits that can function in a variety of frequency bands in order to achieve these requirements. Utilizing Phase-Locked Loops (PLLs) is a useful technique for creating frequency synthesizers. An output signal that is proportionate to the phase of the input signal is produced by a PLL, a type of feedback control system. PL/LL-based on-chip clock generators are the most often used type. The phase frequency detector, charge pump, charge pump, and charge pump is one prominent arrangement of the PLL. The charge pump, phase frequency detector, loop filter, charge pump, and voltage-controlled oscillator (VCO) is one prominent PLL arrangement. The main goal of a PLL is to produce a signal whose phase matches that of the reference signal. After a number of comparison iterations and feedback signal comparisons, it is finished. In lock mode, both the reference and feed-back signal steps are zero. Phase-Locked Loop(PLL) is highly employed for many applications such as smartphones, smart cities, the Internet of Things,large amount of cable connectivity.

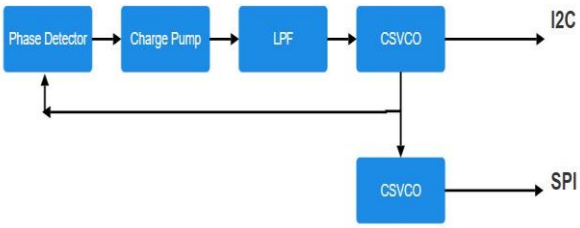

Fig 1 : Block Diagram

In I2C communication, High-Speed Mode (Hs-mode) significantly increases data transfer rates to 3.5 MHz, surpassing Standard and Fast Modes. Hs-mode is activated when a master device sends a special master code followed by a repeated START condition, enabling higher-speed communication on the bus. The Serial Peripheral Interface (SPI) protocol typically uses a clock frequency of 1 MHz, which strikes a balance between speed and reliability for various devices like microcontrollers, sensors, and memory chips. This frequency can be adjusted according to the requirements and capabilities of the master and slave devices, but 1 MHz is a common starting point that ensures stable communication in most SPI implementations.

The objective of this study is to demonstrate the effectiveness of MIMO-OFDM in diverse fading environments and to provide insights into optimizing wireless communication systems for next-generation applications. By evaluating the

interplay between OFDM and MIMO in various channel conditions, this research aimsto contribute valuable knowledge towards advancing the design and deployment of robust and high-capacity wireless networks.

2. Objectives

To design and implement of different blocks of PLL such as phase detector, charge pump, low pass filter, VCO.

To attain frequency for high speed mode of I2C Protocol (3.5MHz) and SPI Protocol(1MHz).

To develop a layout of the design.

3. Methodology

A Phase-Locked Loop (PLL) is a circuit comprising a feedback loop used to lock the frequency and phase of an input signal. The main objective of a PLL circuit is to generate an output signal whose phase and frequency match the reference signal. The input signal provided for locking should have a bandwidth within the lock range of the PLL. The reference clock signal is passed through several blocks and then fed back into the PLL's input as a feedback signal. This feedback loop continues until the phase and frequency of the output signal are locked to the reference signal.

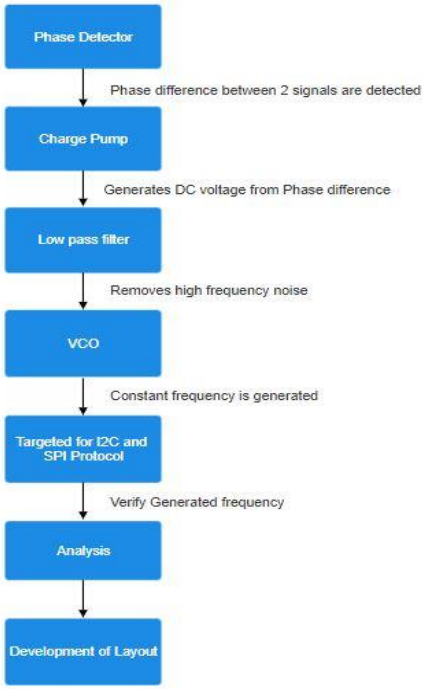

Fig 2 : Design Flow

1. Phase Detector

An essential part of a Phase-Locked Loop (PLL) circuit is a Phase Detector (PD). It does this by comparing the phase of the feedback signal from the PLL's output with the phase of the input reference signal. The phase difference between the two input signals is represented by the output signal produced by the phase detector. In order to maintain the output signal's phase and frequency alignment with the reference signal, this output is subsequently utilized to modify the frequency of the Voltage-Controlled Oscillator (VCO) inside the PLL. By continuously monitoring and correcting any phase discrepancies, the phase detector helps maintain the stability and accuracy of the PLL.There are various types of phase detectors, such as multiplier-based, XOR, JK flip-flop, and Phase-Frequency Detectors (PFDs), each suited to different applications and performance requirements. For example, XOR phase detectors are common in digital PLLs, while PFDs are often used in high-performance PLLs due to their ability to detect both phase and frequency differences, ensuring quick and accurate lock.

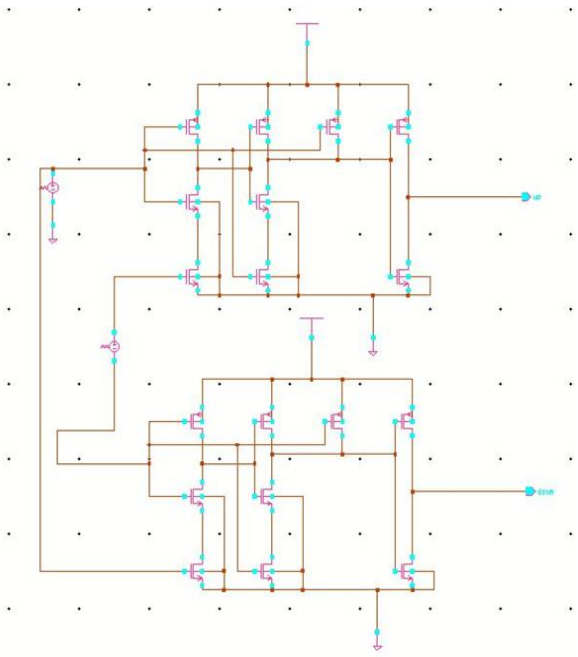

Fig 3 : Phase Detector

2. Charge Pump

A Charge Pump (CP) is a crucial component in a Phase-Locked Loop (PLL), functioning as a DC to DC converter. Positioned between the Phase-Frequency Detector (PFD) and the Low Pass Filter (LPF), the charge pump plays a key role in translating the phase and frequency information

into a control voltage for the Voltage-Controlled Oscillator (VCO). The charge pump generates both positive and negative currents, effectively synthesizing current, and can thus be referred to as a current synthesizer. This ability to generate and regulate voltage directly influences the output frequency of the VCO, ensuring that the PLL maintains lock with the reference signal. The charge pump operates by receiving two input signals (UP and DOWN) from the PFD. The Charge Pump (CP) functions as a type of DC-DC converter within a PLL. It combines the UP and DOWN signals from the Phase-Frequency Detector into a single output signal, which is then sent to the loop filter. The charge pump is composed of two current sources, current mirrors, and PMOS and NMOS transistors that act as switches.

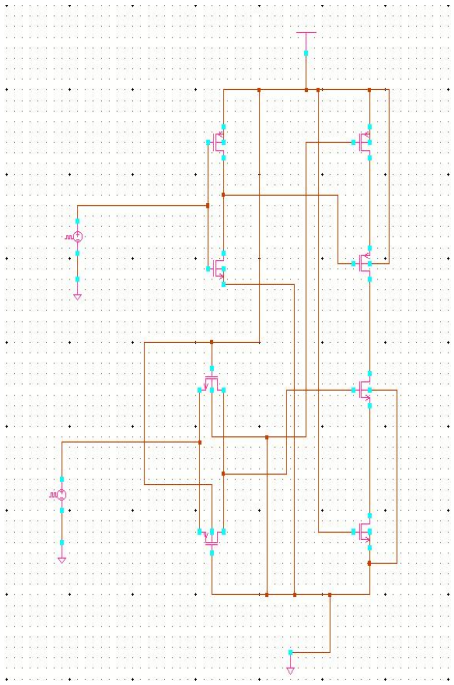

Fig 4 : Charge Pump

These signals indicate whether to increase or decrease the control voltage. The charge pump converts these signals into a single output value, which is then filtered and fed to the VCO. The output voltage generated by the charge pump directly affects the oscillation frequency of the VCO, allowing the PLL to adjust and maintain the desired phase frequency lock.

3. Voltage Controlled Oscillator

The Voltage-Controlled Oscillator (VCO) is a fundamental element in a Phase-Locked Loop (PLL), responsible for converting a DC voltage into a corresponding oscillation frequency. The VCO's output frequency varies proportionally with the control voltage supplied by the Loop Filter (LPF). As the LPF smooths the error signal from the Charge Pump (CP), it adjusts the control voltage applied to the VCO, enabling the PLL to lock onto and stabilize the desired frequency. The ability of the VCO to change its frequency based on this control voltage makes it crucial for maintaining precise synchronization in electronic systems. Among various types of VCOs, the Current Starved Voltage-Controlled Oscillator (CSVCO) is notable for its simplicity and efficiency. The CSVCO uses PMOS and NMOS transistors along with current sources to regulate its oscillation frequency. By controlling the amount of current supplied to the transistors, the CSVCO adjusts its frequency, making it an effective and energy-efficient option. This design allows the CSVCO to cover a broad range of frequencies while maintaining stability and minimizing power consumption.

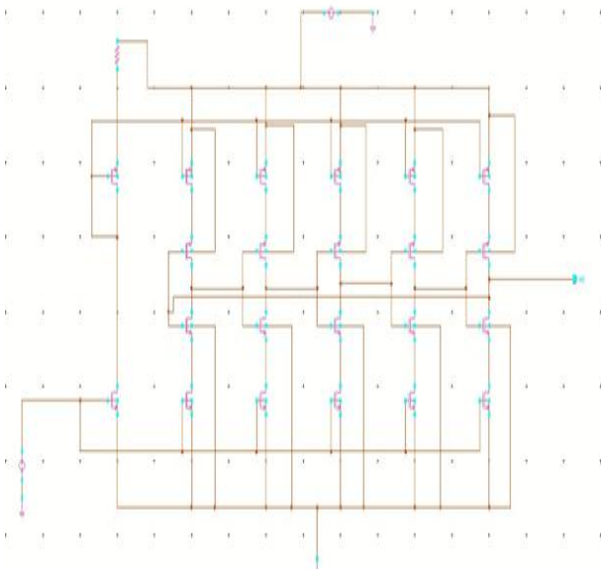

Fig 5 : CSVCO

Due to its straightforward structure and reliable performance, the CSVCO is widely used in communication systems, clock generation for digital circuits, and frequency synthesis applications.

4. Results

Phase Detector Result

When Fref is at a higher frequency than Fvco, the PFD generates a high UP signal and a low DOWN signal. This occurs because the PMOS transistors

responsible for the UP signal are active, while the NMOS transistors that drive the DOWN signal are off, indicating that the VCO frequency needs to be increased to match the higher frequency of Fref.

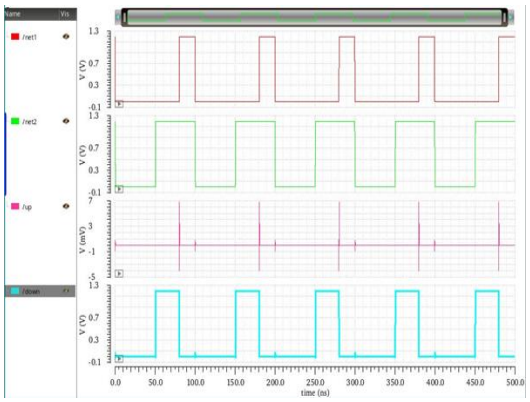

Fig 6 : Slow phase

Conversely, when Fvco is faster than Fref, the DOWN signal is high while the UP signal is low. In this case, the NMOS transistors are active and pull the DOWN signal low, signaling that the VCO should decrease its frequency, as the VCO signal is leading the reference signal. This adjustment process ensures that the PLL aligns the VCO frequency with the reference frequency, achieving synchronization and phase lock.

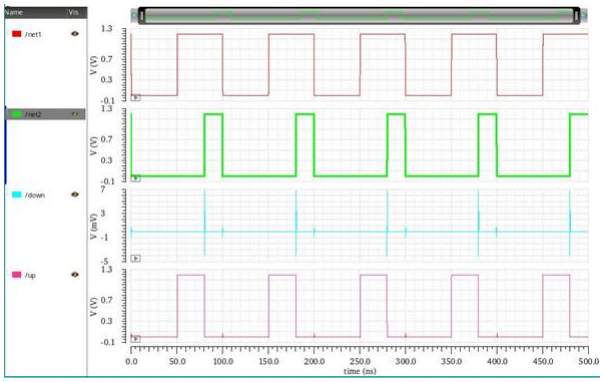

Fig 7 : Fast phase

Charge Pump

When the UP signal from the PFD is high, the Charge Pump generates a positive current, increasing the control voltage applied to the Voltage-Controlled Oscillator (VCO). This adjustment raises the VCO's frequency to better match the higher frequency of the reference signal. Conversely, when the DOWN signal is high, the Charge Pump provides a negative current, reducing the control voltage and thus decreasing the VCO's frequency. This regulation of current is essential for fine-tuning the VCO's frequency, ensuring the PLL remains accurately locked to the reference signal. The effectiveness of the Charge Pump in managing these currents directly impacts the stability and performance of the PLL, influencing its ability to correct frequency discrepancies and maintain synchronization.

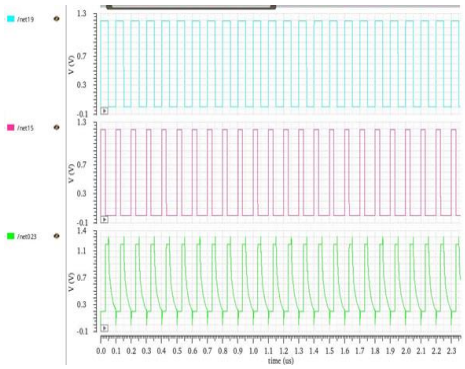

Fig 8 : Charge Pump Output

Voltage Controlled Oscillator

In a communication system supporting multiple protocols such as SPI (Serial Peripheral Interface) and I2C (Inter-Integrated Circuit), employing distinct Voltage-Controlled Oscillators (VCOs) for each protocol is essential for optimal performance. For I2C, particularly in its High-Speed Mode (Hs-mode), the VCO must generate a frequency of up to 3.5 MHz. This high frequency supports faster data transfer rates critical for high-speed communication.

VCO for I2C must maintain stable oscillations with minimal phase noise to adhere to the stringent timing requirements of the protocol. Any deviation in frequency can impact data integrity and communication efficiency, so it is crucial that the VCO provides consistent and reliable performance under various operating conditions.

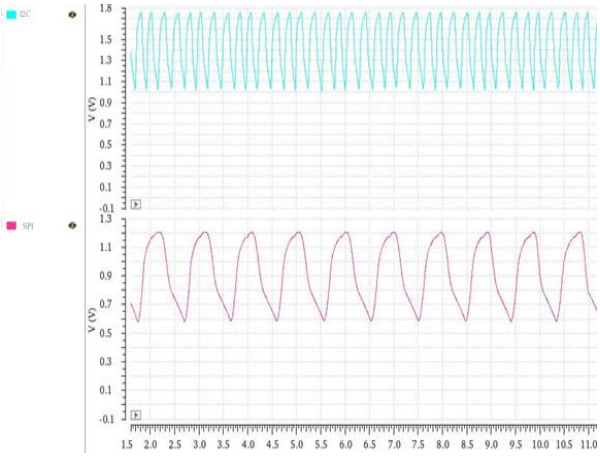

Fig 9 : Two different frequency Output

Communication Protocol	I2C	SPI
Frequency Tuned	3.5MHz	1MHz

Conversely, for SPI communication, which typically operates at a lower frequency of around 1 MHz, a separate VCO is used. This frequency strikes a balance between speed and reliability for standard SPI operations where high-speed performance is less critical. The VCO designed for SPI must ensure stable and accurate low-frequency output, minimizing jitter and drift to ensure reliable communication. By employing specialized VCOs for each protocol, the system can effectively handle diverse communication needs, maintaining performance standards across both high-speed and standard protocols. This separation of VCO functions enhances the overall efficiency and reliability of the communication system, ensuring that each protocol operates within its optimal frequency range.

5. Development of Layout

The layout of the Phase-Locked Loop (PLL) circuit is meticulously crafted to ensure optimal performance and precision in signal processing. Key components such as the Phase Detector (PD), Charge Pump (CP), Loop Filter (LF), Voltage-Controlled Oscillator (VCO), and Frequency Divider (FD) are strategically placed to minimize noise and parasitic elements. The PD and CP are located adjacent to each other to reduce noise coupling and ensure stability, while the LF is positioned between the CP and VCO to smooth the control voltage.

The VCO is centrally placed to minimize noise interference, and the FD is near the VCO to ensure minimal delay and power consumption. Symmetry in the layout is maintained to balance thermal gradients, and dedicated power supply and ground planes are utilized for stable operation. Critical components, especially the VCO, are shielded to maintain signal integrity, with short and wide interconnects used to reduce resistance and inductance. Special attention is given to minimizing parasitic capacitance and inductance through careful placement of components and routing of interconnects.

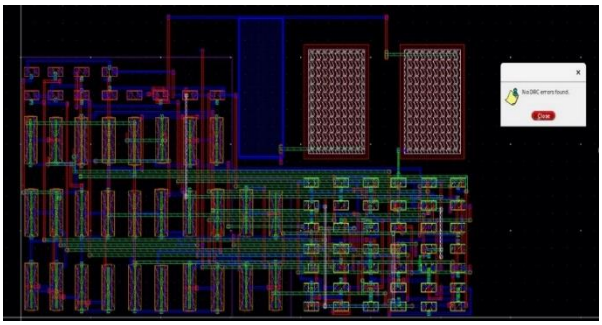

Fig 10 : Layout of the PLL design

The layout undergoes rigorous verification processes, including Design Rule Checking (DRC) to ensure compliance with manufacturing constraints, Layout Versus Schematic (LVS) to verify the layout matches the schematic, and parasitic extraction to identify and mitigate elements that could affect performance. These measures ensure that the PLL circuit operates with high efficiency and accuracy, making it suitable for applications requiring precise frequency synthesis and clock generation.

6. Conclusion

The layout undergoes rigorous verification processes, including Design Rule Checking (DRC) to ensure compliance with manufacturing constraints, Layout Versus Schematic (LVS) to verify the layout matches the schematic, and parasitic extraction to identify and mitigate elements that could affect performance. These measures ensure that the PLL circuit operates with high efficiency and accuracy, making it suitable for applications requiring precise frequency synthesis and clock generation. By employing specialized VCOs for each protocol, the design optimizes performance across varying communication requirements, enhancing the overall efficiency and reliability of the multi-protocol communication system.

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