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A Novel Low Leakage Power Reduction CMOS Design Technique

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Abstract

The paper is based on the idea of new approaches for low- power CMOS circuit design using several techniques in minimizing power consumption and delay. Among these, the Multiple Threshold Voltage (MTCMOS) technique employs the use of transistors with different threshold voltages to allow the circuit to save power by selecting higher threshold voltages whenever full performance is not required. Another technique is Variable Threshold Voltage (VTCMOS), in which threshold voltage is adjusted dynamically according to circuit's operational state. This helps reducing leakage power during inactive states, while ensuring high performance during operational states. In the width modulation method, the width of the transistors is adjusted, which helps optimize both power consumption and performance by balancing the drive strength and leakage current.

The design is simulated using LTspice simulation software based on 90nm, 65nm, and 45nm CMOS Bulk Predictive Technology Models (PTM), which reflect the real-world semiconductor technologies. The results are that the new design approach greatly reduces power consumption, lowers delay, and maintains signal integrity, such that the output signal is still accurate and reliable despite the power-saving techniques. Overall, this novel design method can effectively reduces the power consumption, delay and retain the quality of the output signal in CMOS circuits.

Keywords: cmos, Leakage reduction, Power dissipation.

1. Introduction

Since technology has been advancing highly, circuit design has been made more sophisticated, complex, and advanced. In accordance with Moore's Law, the number of transistors used in electronic circuits has been exponentially growing. As such, sizes of the transistor now declined greatly due to technological advancement for high-density chips. In this respect, the decrease in size led to the issue of increasing the power consumption in CMOS circuits [1,2].

Power dissipation in CMOS circuits may be classified mainly in two category: static and dynamic. The dynamic power dissipation in CMOS circuitry happens through the switching of transistors when the capacitors get charged or get discharged, with the dependency of the activity being on the circuit frequency [3]. However, the steady-state current running through transistors generates the static dissipation of power primarily from leakage currents that flow through these transistors. In addition, total power dissipation in the CMOS circuits is given as the sum of these two powers.

Formerly, designers targeted reduced transistor size for performance. Today, though the transistors continue to be miniaturized, leakage power becomes the dominating portion of total power dissipated. The introduction of leakage has led to a host of problems; the decrease in feature size requires a reduction of supply voltage in order to contain dynamic power dissipation [4]. Reducing supply voltage reduces dynamic power but deteriorates circuit performance by increasing delay. In order to maintain performance both supply voltage and threshold voltage have to be reduced [5], the scaling however incurs a quite

significant increase of leakage currents as a result makes static power dissipation a major challenge in modern CMOS designs [6,7]. The static power dissipation mainly stems from the leakage currents: subthreshold ISUB, gate-induced drain leakage current IGIDL, reverse bias junction IREV and gate oxide tunnelling leakage current IG as shown in figure 1 [8,9]. Altogether, they are considered as the principal components of power dissipation when the transistors do not switch actively.The developed solutions to such issues include power-consumption reduction techniques. They encompass sleep transistors, forced stack methods, variable threshold voltage approaches, and multiple threshold voltage techniques.

This paper will propose a new circuit design technique with the goal of minimizing power consumption in CMOS circuits. It will cover discussion on the current techniques, introduce the proposed method, provide simulation results along with a comparative analysis and conclusions.

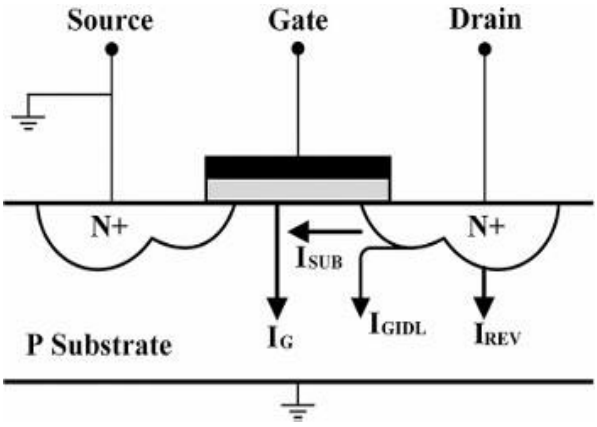

Figure 1: Static leakage current Components

2. Literature Survey

For leakage power reduction, variable threshold CMOS (VTCMOS) and multiple threshold CMOS (MTCMOS) are two popular techniques for reducing leakage power in CMOS circuits by controlling the threshold voltage. In VTCMOS, the threshold voltage of transistors is adjusted using body biasing. When the circuit is active, the substrate terminals are connected to the supply voltage. In active mode, substrate terminals are connected to the supply voltage. During standby mode, threshold voltage is increased by applying substrate voltage higher than the supply voltage for PMOS or lesser than ground for NMOS. VTCMOS circuit diagram is shown in figure2. On the other hand, MTCMOS technique uses sleep transistors with high threshold voltage to reduce leakage power dissipation [10]. MTCMOS circuit diagram is shown in figure3.

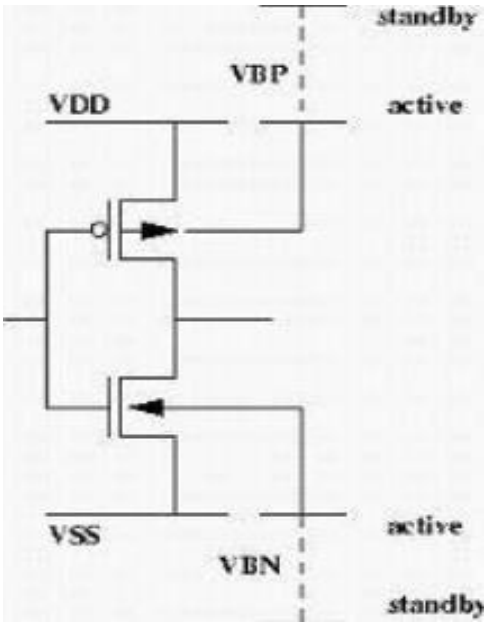

Figure 2: VTCMOS technique

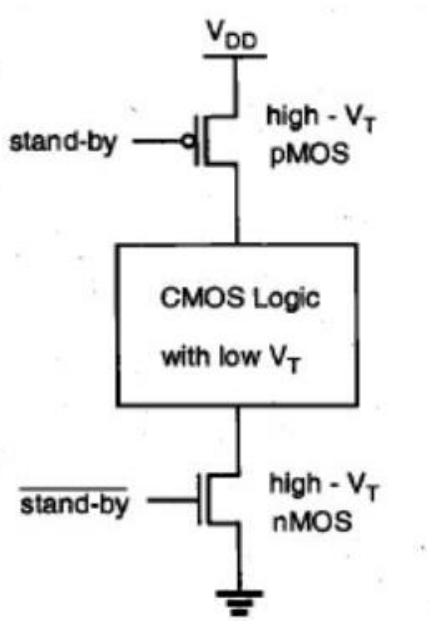

Figure 3: MTCMOS technique

Another popular method of leakage power reduction is sleep transistor technique. Sleep transistors based inverter circuit is shown in figure 4 [11]. In which (M2-M3) is a basic inverter circuit (M1-M4) are sleep transistors. During standby mode, both sleep transistors are turned off which produces large resistance in the conduction path and thus significantly reduces leakage current[12,13]. This technique reduces only standby leakage power and increases area and propogation delay of circuit.

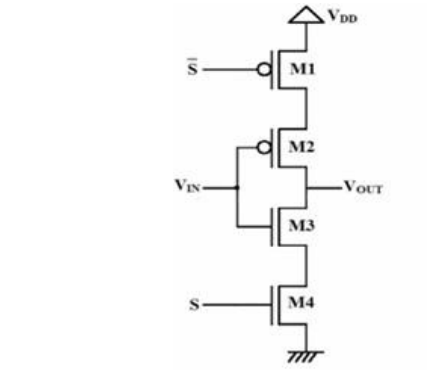

Figure 4: Sleep transistor technique

The forced stack is another technique for leakage power reduction. Here, every transistor with width W is replaced by two transistors with a width of W/2 as depicted in figure 5. This will reduce leakage current as it increases the resistance in the off state, hence lowering the leakage power overall [14]. This technique minimizes the subthreshold leakage current because the resistance is greater when two transistors switched off at a time. This method causes an increase in the area and propagation delay due to additional transistors [15,16].

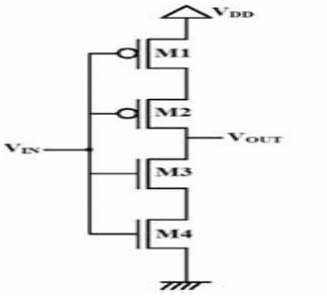

Figure 5. Forced -stack approach

3. Proposed Technique

This section displays a circuit of basic CMOS inverter designed through the proposed approach, as seen in Figure 6. Design The circuit was designed with the connection of two PMOS transistors (M1 and M2) in parallel, while also two NMOS transistors (M3 and M4) were paralleled. This results in connecting the resulting parallel configurations of both PMOS and NMOS transistors in series. Gate terminals of PMOS and NMOS transistors are connected to each other, and the input supply voltage is applied to this connection. The output is obtained from the drain terminals of the PMOS transistors that are connected in parallel.

At time of switching, when supply input voltage is low, the output will be logic high due to M1 and M2 on. If this new method of reducing power is taken into account, it is done by lowering both the input supply voltage and the threshold voltage. This actually reduces the total dissipating power but increases the subthreshold leakage current flowing from source to drain. As the threshold voltage is reduced, the subthreshold leakage current increases substantially and becomes a dominant contributor to the total leakage power of the design.

Conversely, when the input supply voltage is high, both PMOS transistors, M1 and M2, turn off, thus breaking the power supply rail from the ground. When the threshold voltage is lowered, the subthreshold leakage current increases significantly, becoming a major factor in the overall leakage power of design.

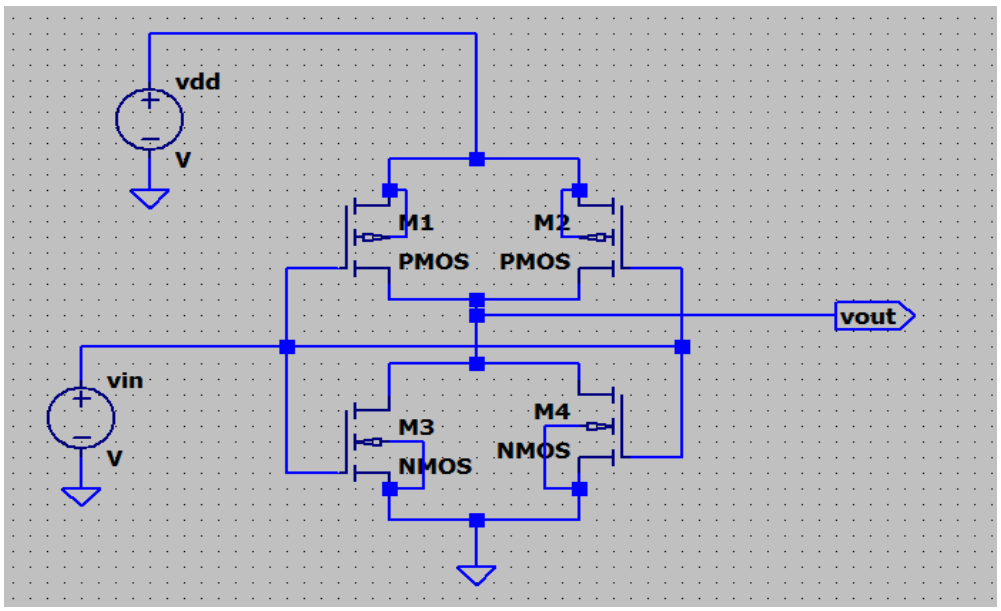

Figure 6: Circuit diagram of proposed technique

4. Results and Comparative Analysis

with a conventional CMOS circuit design considering static power dissipation and propagation delay. Simulation of the designed circuits was carried out using LTspice software employing 90 nm, 65 nm, and 45 nm CMOS bulk PTM model files The proposed circuit design has been compared.

4.1. Static and Transient Response

Figure 7 and Figure 8 show the static and transient responses for the CMOS inverter used with the proposed technique. The input supply voltage changes between 0 and 1.2 V with a swing voltage between 0 and 1.2 V. For the inverter circuit, the output will be logic high when input supply voltage is low, but logic low when input supply voltage is high.

Figure 7: DC characteristics of the inverter circuit using the proposed technique. For low input supply voltage, M1 and M2 PMOS transistors are turned on and provide a conduction path from source to drain. Subthreshold leakage current flows through this path and results in a logic high output. Subthreshold leakage current is the main source of leakage power dissipation in the proposed design. Static power dissipation has been compared across 90 nm, 65 nm, and 45 nm CMOS predictive models, and the graph shows the relationship between input voltage and output voltage.

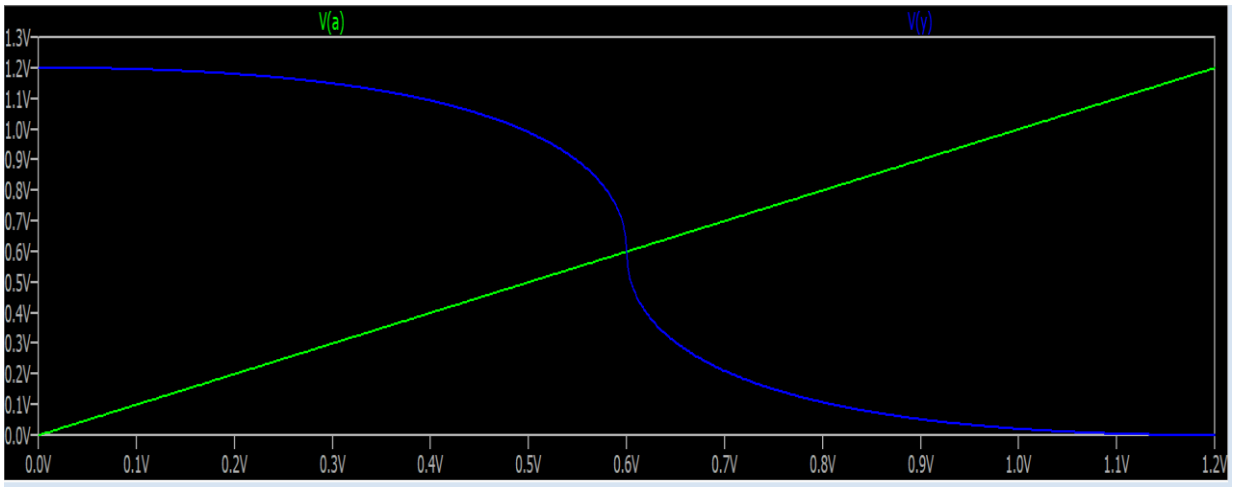

Figure 7: DC characteristics of proposed technique

The transient response of the proposed technique is shown in Figure 8. Propagation delay is computed at the 50% voltage level of switching waveform [16]. This delay represents the time taken for the output to switch states after the input transitions. Specifically, it is measured when the output switches from high to low after an input change from low to high and vice versa.

Overall propagation delay Tpd can be derived as the average of tphl and tplh by the following formula:

$$Tpd = \frac{tphl + tplh}{2}$$

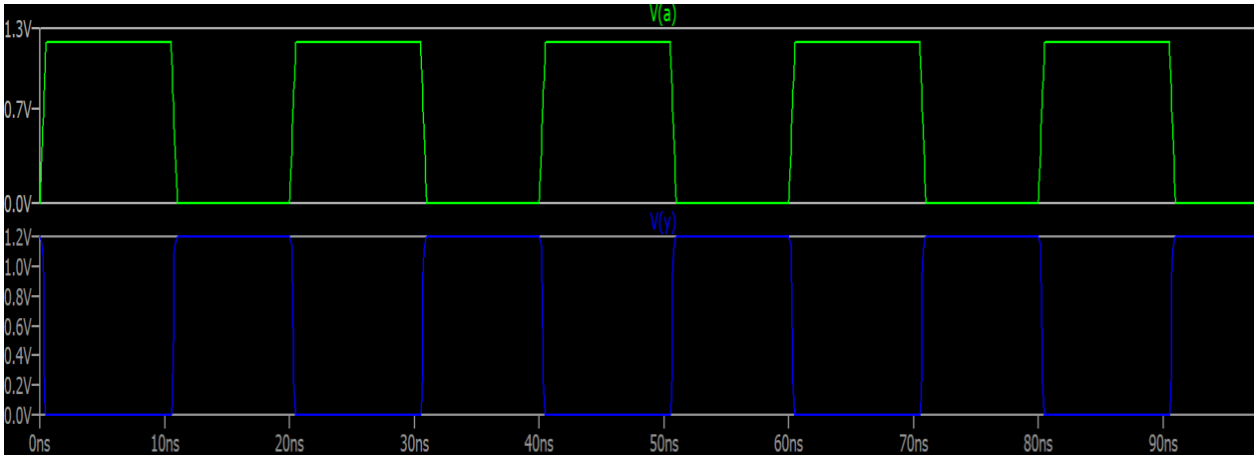

Figure 8: Transient response of proposed technique

4.2. Power and Delay Analysis

The power and delay analysis of the proposed work is summarized through tables. Static power dissipation and delay value for the proposed technique are found in Table 1. Static power dissipation comparison between the proposed design and conventional CMOS is found in Table 2. A comparative propagation delay analysis of the proposed and conventional CMOS is found in Table.

Table1: Static power dissipation and delay calculation of proposed technique

Technology node	Static Power Dissipation	Delay
90nm	5.63nW	0.264ps
65nm	4.41nW	0.319ps
45nm	3.67nW	0.340ps

Static power consumption of the proposed design technique is compared to the CMOS conventional design circuit. For comparison 90nm, 65nm, 45nm PTM Model files are used and results are shown in table 2.

Table2: Comparison of static power dissipation

Technology node	Proposed technique Static Power dissipation	Conventional CMOS Design Static Power dissipation
90nm	5.63nW	18.18nW
65nm	4.41nW	13.87nW
45nm	3.67nW	9.11nW

The static power dissipation of the conventional and proposed technique is listed in a table. Applying the table, it has been reduced at the 90nm technology node by 69.03%. Applying the node of 65nm, it has been reduced by 68.20%, while in the 45nm node, it reduces at 59.71% as compared to the CMOS design of conventional technology. Though the threshold voltage is decreasing in the proposed technique, static power dissipation enhances.

Table 3: Comparison of delay analysis

Technology node	Proposed technique Delay	Conventional CMOS Design Delay
90nm	0.264ns	1.455ns
65nm	0.319ns	1.350ns
45nm	0.340ns	1.237ns

Table 3 Delay comparison of proposed and conventional techniques At 90nm node, the delay is reduced by 82.70%. The delay is reduced by 76.37% for the 65nm node. For the 45nm node, it has been reduced to 72.51%. In other words, delay has decreased in a considerable way, with an important reduction at the 45nm node equal to 72.51%.

Results from the simulations by using 90 nm, 65 nm, and 45 nm PTM model files demonstrate that the proposed design reduces the static power dissipation significantly in comparison to conventional CMOS designs. However, the increase in the number of transistors in the proposed design slightly increases the area and propagation delay. Despite this trade-off, the

reduction in static power dissipation achieved by the proposed technique makes it a valuable improvement over conventional CMOS designs.

5. Conclusion

A novel CMOS circuit design approach aimed at very low power dissipation is introduced. The circuit under study here is a simple CMOS inverter circuit with proposed technique to realize its static power dissipation and propagation delay performance. The outcomes have shown the feasibility of significantly low static power dissipation through the technique; however, an increase in the propagation delay was observed by one extra transistor at each gate stage. Hence, this paper addresses a performance balance where low static power dissipation is a concern, keeping delay characteristics tolerable.

6. Future Scope

Subsequent research may involve optimization methods for minimizing the rise in propagation delay while maintaining low static power consumption. Further, investigating new transistor technologies such as FinFETs or GAAFETs may improve performance and reduce power consumption. Extension of this technique to more sophisticated circuits and systems would be beneficial in assessing its practicality. It is equally crucial to learn about the influence of process and temperature variations on the performance of the design for ensuring reliability at different conditions. This could prove especially helpful in low-power technologies like wearable gadgets, IoT devices, and implantable medical devices, where the power efficiency must be maintained at the highest. The creation of more precise tools for simulation and modeling would help in predicting design behavior at diverse conditions.

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