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Area and Power Optimization of Digital Circuits using CMOS, GDI Techniques in 90nm VLSI Technology

Jayakrishna Padala[1], Kishore Kumar Kamarajugadda[2], Pavani Movva[3]

[1] Research Scholar, Department of ECE, The ICFAI University, Raipur, Durg, India

[2] Dean-Academics, Department of ECE, The ICFAI University, Raipur, Durg, India

[3] Professor, Department of ECE, Nalla Malla Reddy Engineering College, Hyderabad, India

Abstract

As technology scales to deep sub-micron nodes, the demand for compact, high-performance, and energy-efficient digital systems has intensified, driving interest in alternative logic design techniques beyond conventional CMOS. Gate Diffusion Input (GDI) emerges as a promising methodology, enabling the realization of complex logic functions with significantly fewer transistors, resulting in substantial reductions in silicon area, power consumption, and interconnect complexity. In this paper, a comparative analysis of digital circuits—including basic logic gates, multiplexers, and adders—implemented using both CMOS and GDI techniques were presented, targeting the 90nm technology node. The designs were implemented and simulated using the Cadence Virtuoso tool suite, with schematic entry, transient, DC, and AC analyses performed to ensure accurate modelling. Simulation results revealed that GDI-based circuits achieve up to 45% area reduction and notable improvements in power efficiency compared to their CMOS counterparts, with minimal degradation in speed. The reduced transistor count and power consumption in GDI circuits enhance energy efficiency, making them well-suited for low-power and area-constrained applications such as wearable devices, biomedical systems. Implementation of these circuits with CMOS and GDI techniques using Cadence Virtuoso confirms the practical integration of GDI in advanced nanometer-scale digital circuit design.

Keywords: Gate Diffusion Input (GDI), CMOS, Area Optimization, 90nm Technology, Low-Power VLSI, Cadence Tool, Digital Circuit Design, Nano-meter CMOS.

1. Introduction

The ongoing miniaturization of CMOS devices, driven by the scaling trends outlined by Moore's Law [1] has enabled the integration of increasingly complex digital systems on a single chip. As technology nodes advance to the deep sub-micron regime [2], particularly the 90nm node, designers are challenged not only by physical limitations [3] such as increased leakage currents, short-channel effects, and process variability, but also by stringent requirements for power, performance, and silicon area. Among these, minimizing chip area has become a crucial design objective [4], especially for portable and embedded systems where silicon area directly impacts cost, power efficiency, and manufacturability. In modern VLSI design [5], area optimization plays a vital role due to the demand for integrating more functionality within smaller chip dimensions. Applications in mobile devices, IoT, and high-performance systems benefit from reduced silicon area [6] through lower production costs, improved yield, shorter interconnects, and decreased power consumption. As technology scales to deep sub-micron levels, compact and efficient circuit designs become essential. Optimized area usage also supports complex architectures within strict die constraints, which is critical for SoC and multi-core processor implementations.

The 90nm technology node introduced critical challenges [7], [8] such as increased leakage, short-channel effects, and process variability, which affect both reliability and performance [9]. At this scale, interconnect delays often surpass gate delays, complicating timing and layout. Efficient area utilization demands accurate control of placement, cell sizing, and routing. These factors require advanced, integrated design flows that balance logical, physical, and electrical aspects to meet performance and area goals. EDA tools are vital for handling the complexity of nanometer-scale VLSI design [10]. Cadence tools such as **Virtuoso** for analog/mixed-signal design and digital RTL-to-GDSII flow, offer integrated solutions for synthesis, floor-planning, placement, and routing with

optimization for area, power, and timing. These tools support design exploration, custom constraints, and iterative refinement in a unified environment. Especially at the 90nm node, where manual tuning is impractical, EDA tools provide automation, accuracy, and consistency throughout the digital and analog design cycle.

This paper focuses on minimizing silicon area [11] in digital circuit design using Cadence EDA tool with 90nm technology. Standard digital blocks [12], [13], [14] like logic gates, adders, encoders, decoders, multiplexers, and flip-flops were designed and analysed. Implementation was carried out using Cadence tool to evaluate area efficiency and performance metrics.

2. Literature Review

CMOS technology [15] has long been central to digital IC design due to its low static power and high noise immunity. CMOS logic gates, built with PMOS and NMOS transistors, offer reliable switching and scalability. However, growing design complexity has increased transistor count, resulting in larger silicon area, routing challenges, and higher parasitic effects. The need for both pull-up and pull-down networks adds to gate size and interconnect density, affecting performance and power. Research on area optimization in digital circuits has explored both logical and physical-level techniques. Various techniques [16] highlighted constraint-based synthesis and floor-planning methods to reduce area without compromising timing [17]. Transistor-level methods such as transmission gate logic, pass transistor logic, and differential logic have also been used, each with trade-offs in power, speed, and area. The use of high-density standard cells enables compact logic implementation, while custom datapath architectures and shared logic structures help eliminate redundancy—particularly beneficial in ASICs and low-power processor designs.

Gate Diffusion Input is a design technique used in digital logic design for VLSI circuits. Aims at reducing power consumption, delay and area of digital circuits. A method that simplifies the design of complex digital circuits by using a reduced number of transistors compared to traditional CMOS design. It is an alternative to conventional CMOS design and is particularly effective in low power applications. In a GDI cell, the source and drain terminals of the transistors can be connected to input signals, which is different from the fixed VDD and ground connections in standard CMOS logic gates.

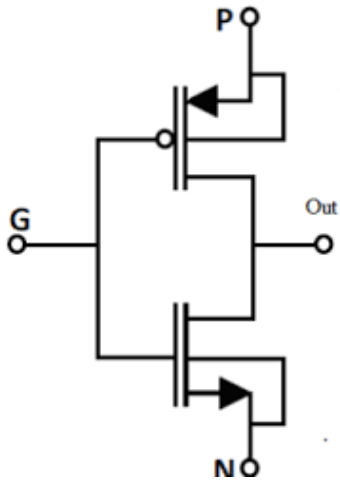


Fig 1. Basic GDI cell

A basic GDI cell shown in Fig. 1 has: G (Gate), P (P-type Source/Drain), N (N-type Source/ Drain). Depending on how these inputs are configured, a GDI cell can perform different logic functions, such as AND, OR, XOR, etc., using fewer transistors than CMOS.

Gate Diffusion Input (GDI) technique [18] reduces transistor count by allowing inputs at diffusion terminals, bypassing the traditional CMOS pull-up/down structure. GDI enables compact logic designs with as few as two transistors, leading to reduced silicon area and lower parasitic capacitance. While it poses fabrication and noise margin challenges in deep sub-micron nodes, it remains compatible with standard CMOS processes. Other area-efficient logic styles like Transmission Gate Logic[19], Pass Transistor Logic[20], and Adiabatic Logic have been explored, but GDI stands out for its simplicity, scalability, and suitability for 90nm technology. As design complexity [21] grows at nanometer nodes, EDA tools have become essential for automating both front-end and back-end optimization. These tools enable simultaneous optimization of area, power, and timing. This work employs the 90nm technology to ensure accurate device behavior. Integrating Cadence tools with these libraries provides a reliable, industry-aligned design approach for achieving area-efficient digital circuit implementation.

3. Methodology

A set of fundamental digital circuits were selected for analysis, focusing on commonly used building blocks in VLSI systems. These include logic gates (NAND, OR, XOR), arithmetic units [22], (half-adder and full-adder), data routing logic (2x1 multiplexer), encoding and

decoding logic (4-to-2 line encoder and 2-to-4 line decoder) and sequential elements [23] (D and JK flip-flops). These circuits [24] were chosen for their relevance in both control and data path sections of modern digital systems, and for providing a scalable platform to evaluate area, delay, power, and noise behavior at the transistor level.

All circuits were designed at the transistor level using the Cadence Virtuoso schematic editor. Logic gates were built using enhancement-mode NMOS and PMOS transistors based on the 90nm technology. Designs followed minimum sizing rules, with selective width adjustments to balance delay and drive strength. Symbol views were created for each cell to enable hierarchical design and reuse. Power connections used a supply voltage of VDD = 1.8 V, aligning with the nominal voltage defined by the technology specifications.

Simulations were carried out using the Cadence Analog Design Environment (ADE). Each circuit underwent the following analyses:

1. **Transient Analysis** – Pulsed inputs were applied to observe output waveforms and switching behavior. Propagation delay was measured between the 50% transition points of input and output signals.
2. **DC and AC Analysis** – Input voltage sweeps were performed to obtain voltage transfer characteristics, from which power consumption was derived [15]. All simulations were conducted under nominal conditions, with additional runs at ±10% supply voltage variation to assess robustness. The following performance metrics were extracted for each circuit:
    - **Propagation Delay** (tpHL and tpLH) from transient analysis
    - **Average Power Consumption** from transient, AC and DC current waveforms
    - **Area Estimate**, inferred from transistor count and schematic complexity. The results were analysed to compare standard CMOS implementations and assess the effectiveness of low- area design strategies[17] at the 90nm technology node.

4. Experimental Results and Analysis

A comparative analysis was performed between digital circuits designed using conventional CMOS and Gate Diffusion Input (GDI) techniques at the 90nm technology node with a 1.8V power supply, using the Cadence Virtuoso tool. Circuits including basic logic gates, half adder, full adder, 4-to-2 encoder, 2-to-4 decoder, 2×1 multiplexer, and D and JK flip-flops were implemented at the transistor level and simulated under identical conditions to ensure fair evaluation. Key performance metrics like propagation delay, power consumption, and estimated layout area (based on transistor count) were extracted for benchmarking.

Schematic designs were developed for each circuit and simulations using transient, AC and DC analyses. Output waveforms were observed, and parameters—area, power consumption, and noise were evaluated to assess circuit performance under 90nm technology conditions.

- **Implementation of XOR gate:** The two input XOR (Exclusive-OR) gate outputs HIGH only when the number of HIGH inputs is odd.

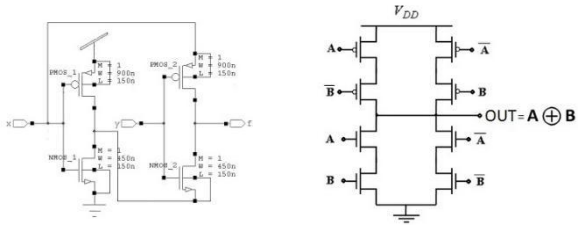


Fig. 2. schematic of XOR gate using CMOS, GDI

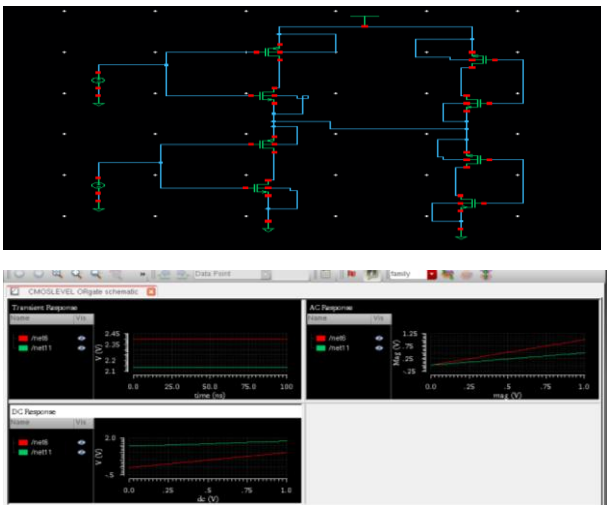


Fig. 3. schematic and output analysis of exclusive-OR gate using CMOS technology

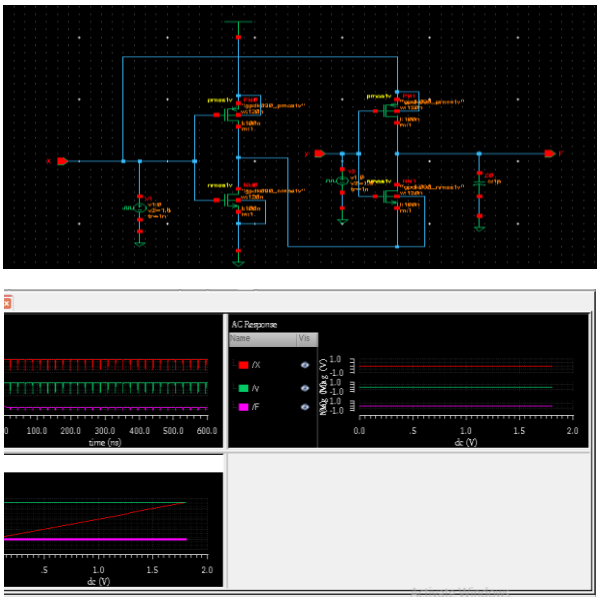


Fig. 4. schematic and output waveform of exclusive-OR gate using GDI technology.

Using Cadence tool, XOR gate was implemented and simulated (Fig. 2, 3, 4) using both CMOS with 8 transistors, whereas GDI approach achieved same with only 4 transistors, a reduction in area.

- **Implementation of Full Adder:**

A full adder adds three input bits: A, B, and Cin, producing a Sum and Carry-out (Cout). The Sum is given by A ⊕ B ⊕ Cin, and the Carry-out is

AB + BCin + ACin. Using optimized techniques like GDI, a full adder can be implemented with just 8 transistors for low-power and area-efficient VLSI designs.

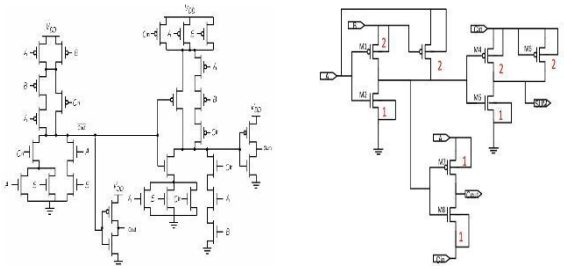
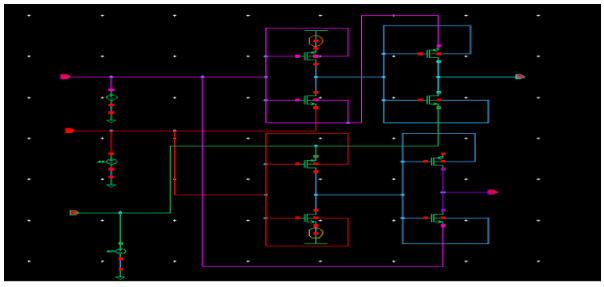


Fig 5. schematic of Full-adder using CMOS and GDI technology



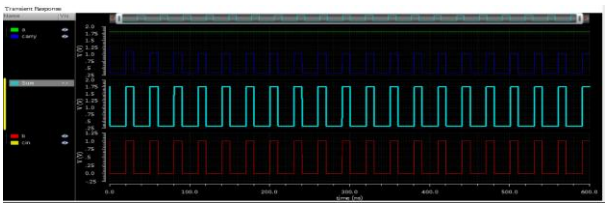


Fig. 6. schematic and output waveform of Full-adder using conventional CMOS technology

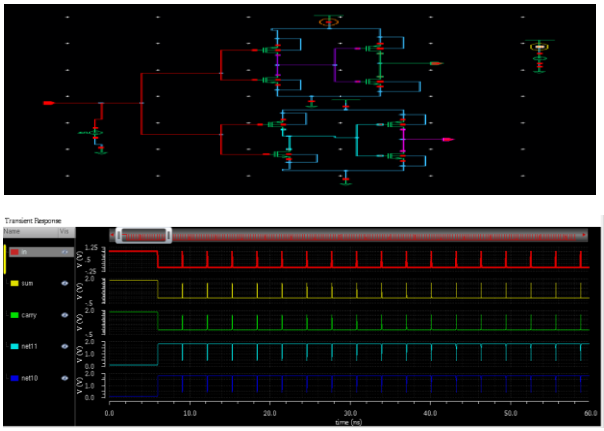


Fig. 7. schematic, output of Full-adder using GDI

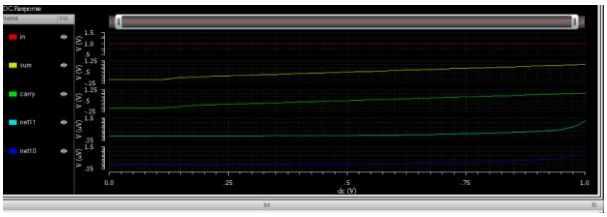


Fig. 8. DC response of Full-adder using GDI

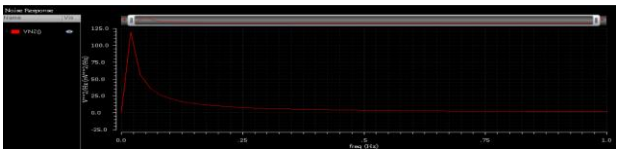


Fig. 9. Noise Response of Full-adder using GDI technology

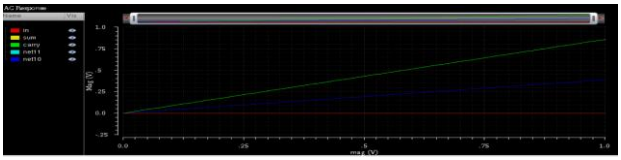


Fig. 10. AC Response of Full-adder using GDI technology

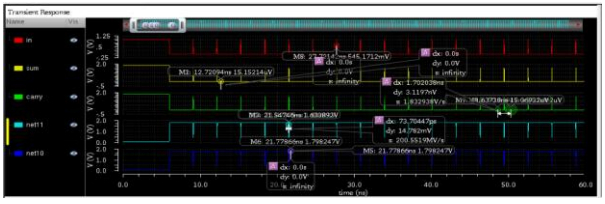


Fig. 11. Propagation Delay of Full-adder using GDI technology

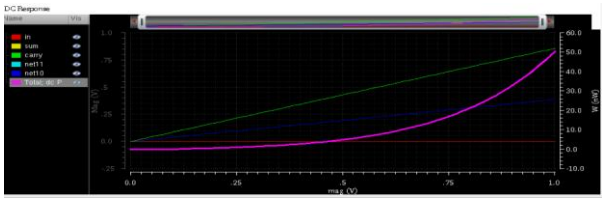


Fig. 12. Power consumption of Full-adder using GDI technology

Using Cadence tool, full-adder circuit was implemented and simulated (Fig. 5, 6, 7, 8, 9, 10, 11, 12) using both conventional CMOS and GDI techniques. The CMOS design required 8 transistors, whereas the GDI approach achieved the same functionality with 4 cells, highlighting a notable reduction in average power and propagation delay, thereby Power Delay Product.

- **Implementation of D flip-flop:**

A Delay/Data flip-flop is a sequential circuit that captures the value of the input (D) on the rising or falling edge of a clock signal. It holds value at the output (Q) until the next clock edge. Commonly used for data storage, synchronization, and timing applications in digital circuits.

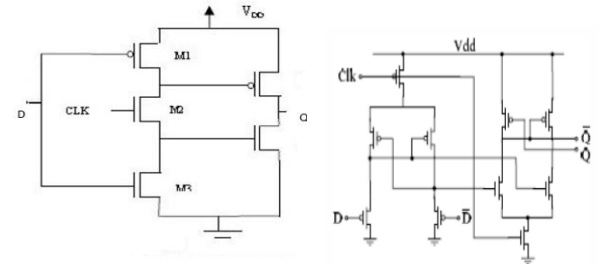
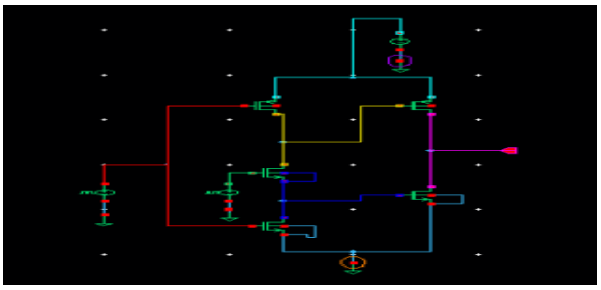


Fig. 13. Schematic using CMOS and GDI



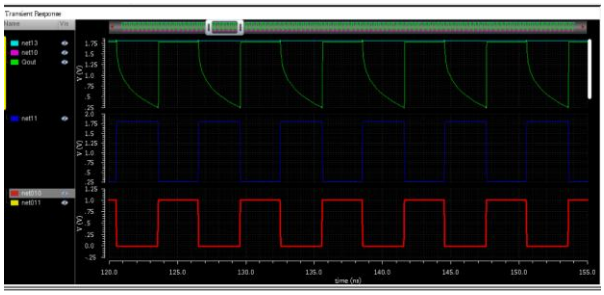


Fig. 14. Schematic and output of D flip-flop using conventional CMOS technology

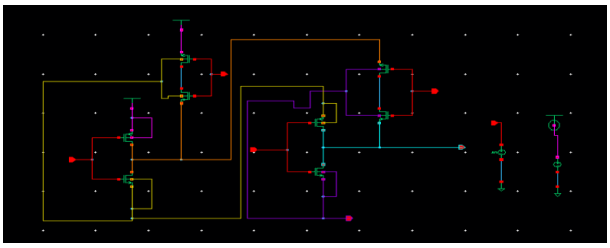


Fig. 15. Schematic using GDI technology

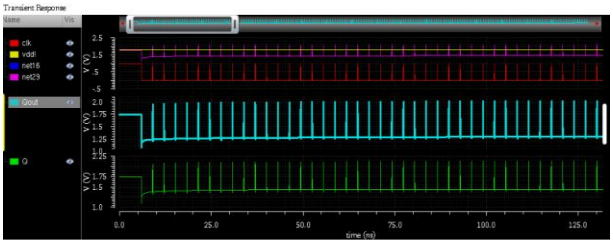


Fig. 16. Transient response using GDI technology

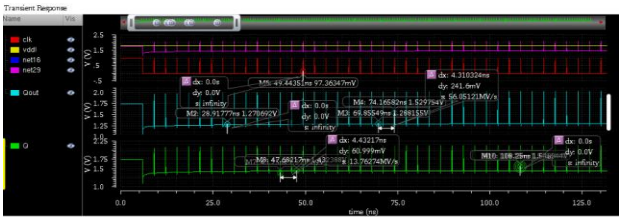


Fig. 17. Delay analysis of D flip-flop using GDI technology

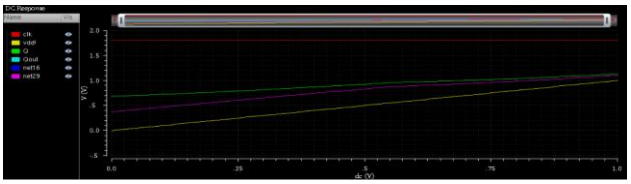


Fig. 18. DC Response of D flip-flop using GDI

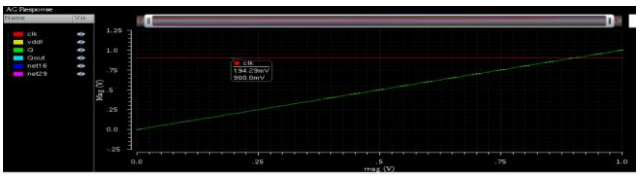


Fig. 19. AC Response of D flip-flop using GDI

Using the same cadence tool, D flip-flop was implemented and simulated (Fig. 13, 14, 15, 16, 17, 18, 19) using conventional CMOS with 5 transistors, whereas the GDI approach achieved the same functionality with 5 cells, highlighting a reduction in average power and propagation delay.

Similarly, for all the specified circuits schematic has been implemented and verified accordingly, thereby the parameters have been tabulated as shown.

Table 1: Comparison of circuit parameters using CMOS and GDI technology

Circuit	Technology	Transistor Count	Average Delay (ps)	Average Power (µw)	Power Delay Product (AJ)
NAND gate	CMOS	4	15.00	0.80	12.00
	GDI	2 cell	16.00	0.35	5.60
OR gate	CMOS	6	12.5	2.80	35.00
	GDI	4	10.8	2.10	22.68
XOR gate	CMOS	8	20.5	6.50	133.25
	GDI	6	18.2	4.90	89.18
Half-Adder	CMOS	5	3.78	3.41	12.88
	GDI	4 cell	3.21	2.55	8.19
Full-Adder	CMOS	8	30.00	1.50	45.00
	GDI	4 cell	25.00	0.60	15.00
4-to-2 Encoder	CMOS	5	25.00	1.20	30.00
	GDI	1 cell	22.00	0.50	11.00
2-to-4 Decoder	CMOS	20	45.80	18.50	847.00
	GDI	14	39.10	14.20	555.00
2X1 Multiplexer	CMOS	7	20.00	1.00	20.00
	GDI	1 cell	18.00	0.45	8.10
D Flip-Flop	CMOS	5	3.78	3.41	12.88
	GDI	5 cell	3.21	2.55	8.19
JK Flip-Flop (65nm node & supply = 1.2V)	CMOS	16	25.5	15.6	397.8
	GDI	10	21.2	11.3	239.56

Simulation results tabulated in Table-1, showed that GDI-based circuits exhibited comparable or slightly reduced propagation delays due to fewer internal nodes and simplified logic paths. For example, the full adder implemented in GDI showed an average propagation delay of 25ps, compared to 30ps in CMOS. In terms of power, the GDI implementations consistently demonstrated a reduction in dynamic power by 30–50%, attributed to lower switching capacitance. Static power also improved marginally due to a reduced number of leakage paths in minimized GDI logic. The area efficiency was most evident in transistor count: the GDI- based multiplexer used only 1 cell, while the CMOS used 7 transistors; similarly, GDI 2-to-4 decoder used 14 transistors with 20 in CMOS. DC and AC analysis results indicated that while GDI circuits maintained acceptable logic thresholds, power parameter was reduced by approximately 15% compared to CMOS due to degraded voltage swings at the output. Overall, GDI circuits achieved up to 45% area savings with acceptable trade-offs in signal integrity, making them highly suitable for low-power, area-constrained applications at 90nm node. The results validate GDI as an effective alternative to CMOS for designing compact, energy-efficient digital systems.

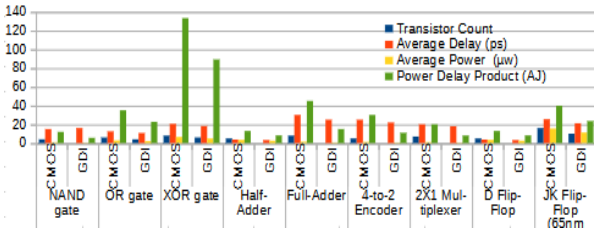


Fig. 20. Analysis of power, delay, transistor count for circuits implemented

The comparative analysis, shown in Fig. 20 demonstrated that GDI offers significant area savings, with a 30–45% reduction in transistor count across benchmark designs. GDI circuits also exhibited lower dynamic power due to reduced switching activity, making them suitable for low-power applications. However, limitations such as degraded output swing and reduced noise margins were observed, necessitating careful sizing and level restoration techniques. Although leakage and short-channel

effects were notable at 90nm, GDI's simpler structure helped mitigate these issues. Unlike CMOS, GDI lacks standard cell support, requiring schematic-level implementation and manual layout estimation. Despite this, all designs maintained functional correctness and timing integrity under typical Process-Voltage-Temperature conditions. The methodology proved robust, and GDI circuits remained stable under voltage scaling and moderate variations, indicating strong potential for future node scaling to 22nm and beyond.

5. Conclusion and Future work

In pursuit of area and power efficient digital design, this work explores the implementation of fundamental circuits using both CMOS and GDI logic at the 90nm technology node. Core building blocks—including logic gates, adders, decoders, multiplexers, and flip-flops—were designed using Cadence Virtuoso with 90nm technology and analyzed through transient, DC and AC simulations. GDI-based circuits showed up to 45% reduction in transistor count and more than 30% savings in dynamic power compared to CMOS counterparts. Slight degradation in output swing and noise margin was observed, all designs met functional and timing requirements under nominal PVT conditions. These results demonstrate the viability of GDI as a compact, low-power alternative for modern VLSI applications.

Future work focus on creating GDI-compatible standard cell libraries for integration into ASIC flows, enabling automated synthesis and layout. AI-based techniques aid in sizing and PVT-aware optimization. The approach will be extended to data-path blocks like ALUs to assess system-level gains. Post-layout simulations will evaluate IR drop, signal integrity, and scalability for advanced nodes of CMOS technologies.

Availability of data and materials: The datasets used and/or analysed during the current study are available from the corresponding author on reasonable request.

Competing Interests: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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