

Design and Implementation of Mixed Signal Measurement System Using FPGA

¹ M Kiran, ² Mrs. Shrisha M R,

Department of Electronics & Communication Engineering

¹ Student, BMS College of Engineering, Bangalore

² Assistant Professor, BMS College of Engineering, Bangalore

Abstract

This project presents the design and implementation of a measurement system using a Field-Programmable Gate Array (FPGA) and an Analog-to-Digital Converter (ADC) to process mixed-signal inputs and perform a variety of signal measurements. The system is capable of accurately measuring essential parameters of the input signal, such as voltage levels, 8 bit parallel digital data and 8 bit serial digital data (in formats like hexa decimal or Binary). The FPGA is responsible for the real-time processing of the signals and the extraction of these measurements, leveraging its parallel processing capabilities to ensure high-speed performance. The system integrates a USB-to-UART interface for communication between the FPGA and a personal computer. This interface enables the transmission of the measured data to the PC, where it can be displayed and analyzed via a user-friendly graphical interface. The measured values, including voltage, digital input are presented on the PC in an easily interpretable format, allowing for real-time monitoring and evaluation of the input signal.

Keywords: Mixed-signal measurement system, FPGA, ADC, UART, real-time monitoring, signal analysis, digital data acquisition.

1. Introduction

Measurement systems plays crucial role in scientific research, engineering, industrial processes and everyday applications. These systems are designed to observe, analyze, and quantify physical or electrical parameters such as voltage, current, temperature, pressure, frequency, and time. At their core measurement systems bridge the gap between the physical world and digital analysis by converting real-world signals into interpretable data. Modern measurement systems often consist of sensors or transducers, signal conditioning circuits, data

converters (e.g., ADCs), processing units, and output interfaces. With advancements in technology, these systems are now equipped with higher accuracy, better resolution, faster processing, and greater flexibility. Measurement systems are widely used in areas such as electronics testing, biomedical instrumentation, industrial automation, and communication networks, making the min dispensable in ensuring product quality system reliability, and operational efficiency. This project involves in the design and implementation of an FPGA-based measurement system integrated with an ADC to analyze mixed signals. The system can

measure essential parameters such as voltage levels, data in binary or hexadecimal formats. The FPGA, acting as the core processing unit, enables real-time analysis, high-speed data processing, and adaptability to various signal types. The ADC digitizes the analog components of the input signal, ensuring accuracy during measurement. The extracted data is transmitted to a PC via a USB-to-UART interface, allowing for a user-friendly display and analysis of the measured parameters.

This project leverages the reprogrammable nature of FPGAs and the precision of ADCs to provide a versatile and scalable solution for signal measurement challenges. It is well-suited for applications in industries such as electronics, telecommunications, and automation, where precise signal analysis is critical. Few of the uses of our proposed project is that Engineers can use this system to analyze and debug circuits by measuring signal characteristics like voltage levels and frequencies accurately, Real-time monitoring of signal outputs from machines can ensure operational efficiency and timely maintenance, In education system the system can be used as a teaching and research tool to demonstrate and study signal measurement techniques and FPGA-based designs, In communication system the project can monitor and validate signals in communication devices, ensuring proper functioning and signal integrity, In healthcare system adapted versions can measure and analyze bio-signals like ECG or EEG for diagnostic purposes.

The novel contribution of this work lies in its ability to simultaneously perform both analog and digital signal acquisition within a single, integrated FPGA-based framework, making it a unified solution for comprehensive mixed-

signal analysis.

Future scope of the proposed project is the system can be upgraded to include advanced signal processing capabilities, such as spectrum analysis, edge detection, or noise filtering, Future versions can support the simultaneous measurement of multiple input signals, making it suitable for more complex systems by incorporating IoT capabilities, the system can transmit measured data to cloud platforms for remote monitoring and predictive maintenance. Integrating AI algorithms can enable the system to detect anomalies, classify signals, or predict potential faults in real-time.

2. Objectives

The primary objective of this project is to develop a mixed-signal measurement system capable of capturing and analyzing both digital and analog input signals simultaneously. For digital signal acquisition, the system supports two modes: 8-bit parallel data input and 8-bit serial data input, with logic levels defined such that 0V represents a logical LOW and 5V represents a logical HIGH. For analog signal acquisition, the system is designed to accurately measure voltage levels ranging from 0 to 5V with an accuracy of 100mV. The analog input is interfaced to the FPGA using an ADC via the SPI protocol, enabling precise conversion of real-world signals into digital data. Communication between the FPGA and the PC is established through a UART interface, allowing real-time transmission and display of both digital and analog data on a PC terminal. The system is designed to present digital data in both binary and hexadecimal formats, while analog voltage values are displayed with appropriate resolution,

ensuring clarity and ease of interpretation for users.

3. Methods

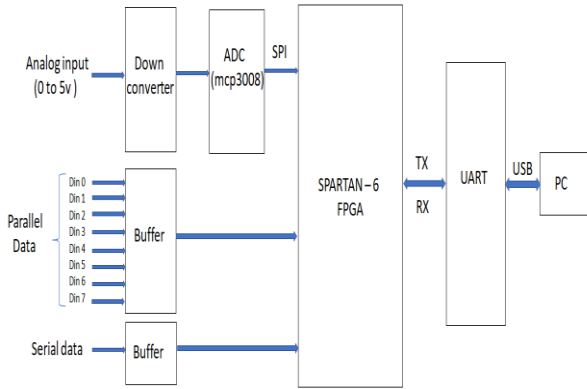


Fig1: Block Diagram of mixed signal measurement system

DIGITAL SIGNAL ACQUISITION

The methodology of this project revolves around the implementation of transmitter and receiver modules to enable communication through a terminal interface. The system responds to user inputs to perform specific tasks. When the user presses the "I" key, the transmitter sends a predefined message to the terminal, confirming successful communication. If the user presses "R", the system captures 8-bit parallel data from eight designated input pins simultaneously and then transmits this collected data back to the terminal for display. Alternatively, when the user presses "r", the system captures 8-bit serial data from a single input pin, bit by bit, before transmitting the complete byte to the terminal. This structured approach ensures flexible and interactive data handling, demonstrating the functionality of both parallel and serial data acquisition using the developed UART communication modules.

The system uses a Universal Asynchronous Receiver Transmitter (UART) protocol for serial communication between devices. This protocol operates using just two signal lines: one for transmitting (TX) and the other for receiving (RX). Data is transmitted asynchronously in a frame-based format, which allows two devices to communicate without a shared clock signal. Each UART frame consists of a start bit, followed by data bits, an optional parity bit, and a stop bit. The line remains high during idle states. A start bit—represented by a low signal—indicates the beginning of a transmission. Once the data has been sent, a stop bit—represented by a high signal—marks the end of the frame. This structure enables consistent and efficient communication, even over simple hardware setups.

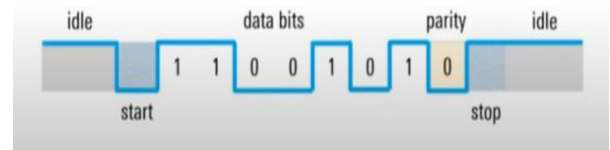


Fig2: UART Frame Format

Since UART operates asynchronously, the transmitter and receiver do not share a common clock signal. Instead, both devices must be configured to transmit and receive data at the same predefined speed to ensure proper communication. This characteristic eliminates the need for clock synchronization lines, simplifying hardware design while maintaining reliable data exchange. In the proposed FPGA-based signal measurement system, the UART interface has been configured to operate at a baud rate of 115200 bits per second, balancing ease of implementation with sufficient data throughput for real-time signal control and monitoring.

Common UART baud rates
4800
9600
19200
57600
115200

Fig3: Baud Rate

The transmitter and receiver in the proposed FPGA-based signal measurement system are modelled using finite state machines to ensure accurate UART communication.

The UART transmitter operates through a sequence of states: Idle, Start, Transmit, and Stop. In the Idle state, the system continuously monitors the RX line, waiting for a specific input character, such as "R", "r", or "I", to initiate communication. Once a valid character is received, the transmitter moves to the Start state, where the start bit is transmitted by setting the TX line low (TX = 0) at the predefined baud rate. Following the start bit, the system transitions to the Transmit state, where each data bit is sequentially sent over the TX line, also adhering to the known baud rate. After transmitting all eight bits of the data frame, the system proceeds to the Stop state, where a stop bit is transmitted by setting the TX line high (TX = 1). Upon completion of the stop bit transmission, the transmitter returns to the Idle state, ready to handle the next incoming data frame.

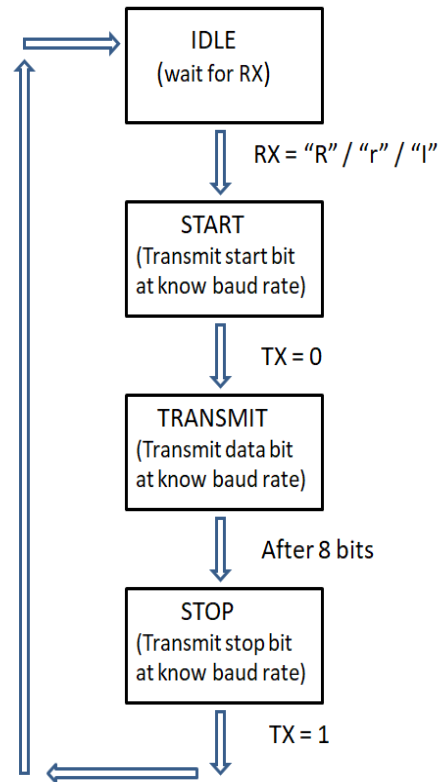


Fig4: State diagram of transmitter

The UART receiver operates through three primary states: Idle, Receiving, and Validate. In the Idle state, the system continuously monitors the RX line, waiting for the detection of a start bit, indicated when RX goes low (RX = '0'). Upon detecting the start bit, the receiver transitions to the Receiving state, where it begins sampling incoming bits at the predefined baud rate. It collects a total of 10 bits, which include the start bit, eight data bits, and the stop bit. After all 10 bits have been received, the system moves to the Validate state, where it checks the correctness of the stop bit to ensure the integrity of the received data. If validation is successful, the receiver outputs the captured data and returns to the Idle state, ready for the next incoming transmission.

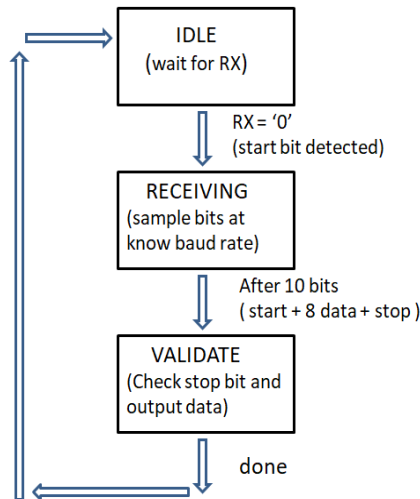


Fig5: State diagram of receiver

ANALOG SIGNAL ACQUISITION

The analog signal acquisition in this system is accomplished using the SPI (Serial Peripheral Interface) protocol. SPI is a high-speed, full-duplex, synchronous communication protocol commonly used for short-distance data exchange between a master and one or more slave devices. In this project, the Spartan-6 FPGA acts as the SPI master while the MCP3008 ADC serves as the SPI slave. The SPI communication involves four main lines: Chip Select (CS), Serial Clock (SCLK), Master Out Slave In (MOSI), and Master In Slave Out (MISO).

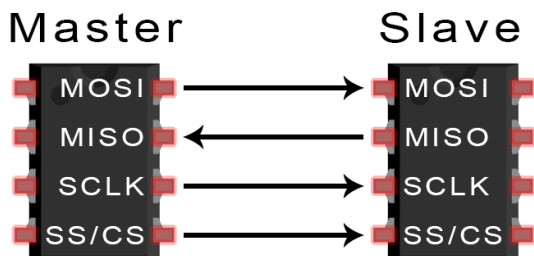


Fig6: SPI protocol connection

The SPI communication process follows a defined sequence when the FPGA initiates data conversion. First, the Chip Select (CS) line is pulled LOW by the FPGA to activate the MCP3008. Then, command bits are sent

through the MOSI line to choose the ADC channel and select either single-ended or differential mode. Once the configuration is received, the MCP3008 samples the analog input, performs the conversion internally, and transmits the 10-bit digital result back to the FPGA via the MISO line. All data is exchanged synchronously with clock pulses generated by the FPGA on the SCLK line. After receiving the necessary bits, the FPGA deactivates the communication by pulling CS HIGH.

The SPI communication is further explained through a state diagram, which includes the following steps: The system starts in the IDLE state with CS HIGH. When CS goes LOW, it becomes active, and a start bit (logic 1) is sent over MOSI. Upon receiving the start bit, configuration bits (SGL/DIFF and channel selection) are sent. Once these bits are received, the MCP3008 performs internal sampling and conversion. The resulting 10-bit digital output is then shifted out through the MISO line, and finally, CS is pulled HIGH again, returning the system to the IDLE state.

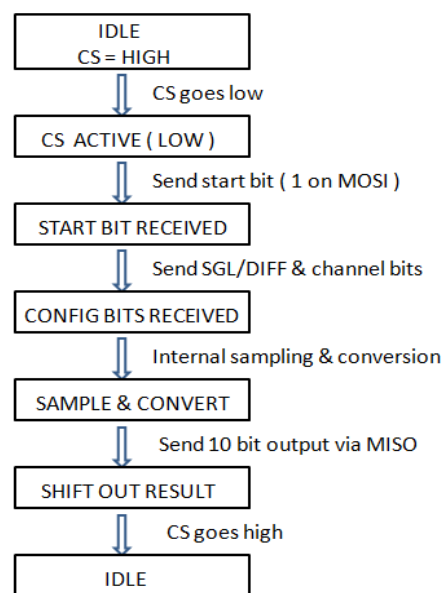


Fig7: State diagram of analog signal acquisition

To handle analog input signals that may have higher voltage levels such as +5V or +15V, signal conditioning is performed using dedicated down converters. These converters bring the signal voltage within the range compatible with the ADC, ensuring both accurate signal acquisition and protection against high voltage levels. After conditioning, the analog signals are input to the MCP3008, which operates as a Successive Approximation Register (SAR) ADC. The SAR ADC is responsible for converting the analog signals to their digital equivalents, making them suitable for FPGA processing. The digitized output from the ADC is then processed by the FPGA. The FPGA is programmed to calculate important signal parameters such as voltage levels using custom logic and algorithms. Its parallel processing capabilities allow real-time data computation with high accuracy. Additionally, DDRAM is used alongside the FPGA for effective data storage and handling during processing. Once the computation is complete, the processed data is sent to a PC using a USB-to-UART interface. This module plays a crucial role as a communication bridge between the FPGA and the personal computer (PC), facilitating seamless data exchange. It is specifically designed to convert the electrical output signals generated by the FPGA into a USB-compatible data format, making it interpretable and readable by the PC's operating system and application software. This conversion ensures reliable communication and allows the PC to effectively receive and process data transmitted from the FPGA. Once the data is received by the PC, it is typically displayed through a user-friendly graphical interface or terminal software, enabling users to easily

visualize and interpret the measured parameters. This intuitive presentation of data supports quick understanding and efficient analysis of the signal characteristics or results obtained from the measurement system.

4. Results

DIGITAL SIGNAL ACQUISITION

8-Bit Parallel Digital Data:

Input Data: 0x31

For input Data 0x31 the binary Value is "00110001"

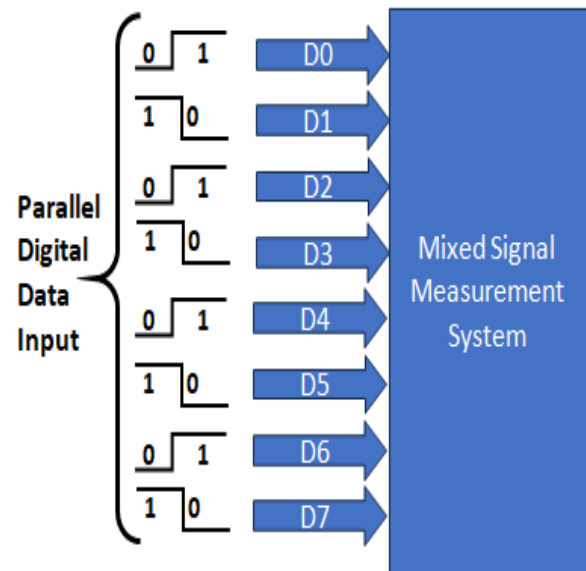


Fig8: Overview of 8 bit parallel digital signal acquisition

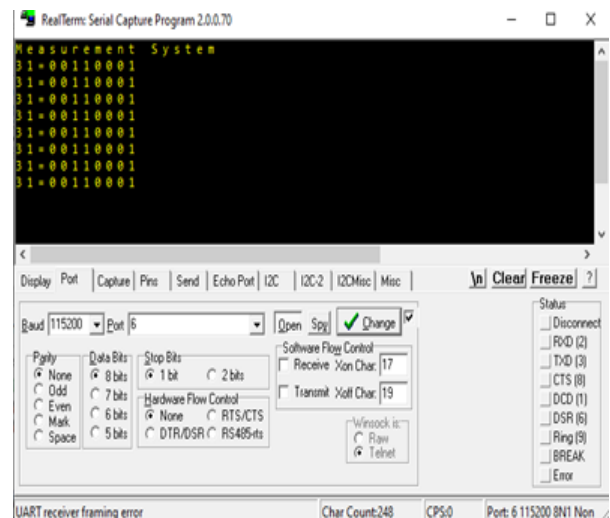


Fig9: 8 bit parallel digital signal acquisition over serial terminal

8-Bit Serial Digital Data:

Input Data: 0x19

For input Data 0x19 the binary Value is "00011001"

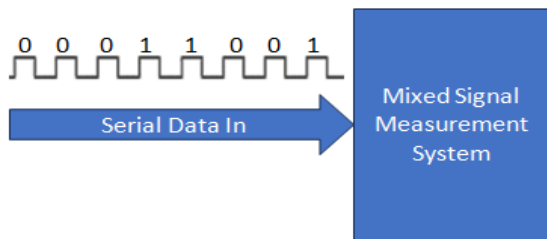


Fig10: Overview of 8 bit serial digital signal acquisition

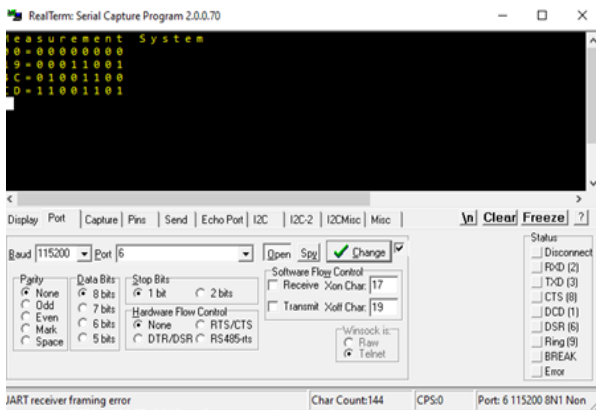


Fig11: 8 bit serial digital signal acquisition over serial terminal

ANALOG SIGNAL ACQUISITION

Input data: 2.4v

For input Data 2.4v the binary value is "0111101011"

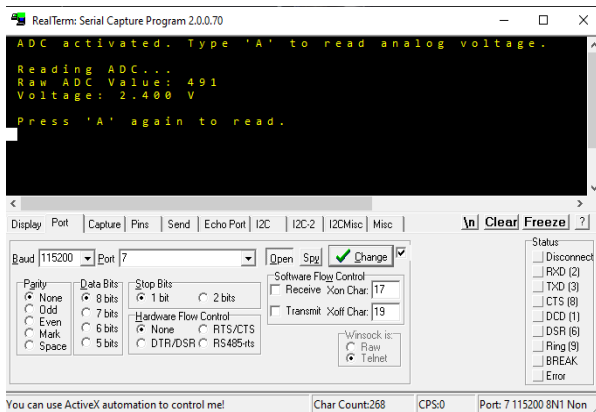


Fig12: Analog signal acquisition over serial terminal

Input data: 2.6v

For input Data 2.6v the binary value is "1000010100"

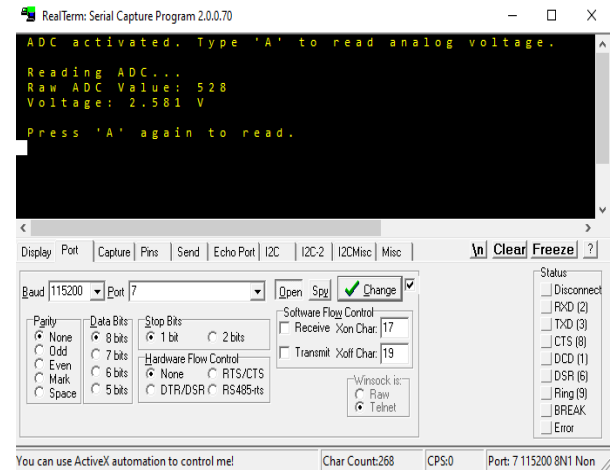


Fig13: Analog signal acquisition over serial terminal

5. conclusion

This paper presented the design and implementation of a mixed-signal measurement system using an FPGA in conjunction with an ADC. The proposed system effectively acquires both digital and analog inputs, processes them in real-time, and transmits the results to a PC using UART communication. For digital signals, both 8-bit parallel and serial data acquisition techniques were demonstrated, while analog signals were processed through an SPI-based interface with the MCP3008 ADC, ensuring accurate conversion and analysis.

The use of an FPGA enables high-speed data handling, flexible system control through finite state machines, and adaptability for various applications. Real-time monitoring and result visualization on a PC further enhance the system's usability for debugging, industrial monitoring, and educational purposes. The modular design also allows for

scalability and integration into larger systems.

Future developments can incorporate advanced signal processing algorithms, AI-based diagnostics, and cloud connectivity for remote monitoring, making the system highly versatile for next-generation embedded measurement solutions.

References

- [1] N. Corna, F. Garzetti, N. Lusardi and A. Geraci, "Digital Instrument for Time Measurements: Small, Portable, High-Performance, Fully Programmable," in *IEEE Access*, vol. 9, pp. 123964-123976, 2021, doi: 10.1109 / ACCESS.2021.3109155.
- [2] Yongfu Xiao, Hao Zhang and Hao Zou, (2020) "Design of a Quad-Channel Analog Data Acquisition System Based on FPGA," in *Open Access Library Journal*, vol. 7, pp. 1-6, doi: 10.4236/oalib.1107058.
- [3] W. Han, Y. Hu, M. Shi, X. Lin and P. Zou, "Design of High Precision Data Acquisition System Based on FPGA," 2024 5th International Conference on Artificial Intelligence and Electromechanical Automation (AIEA), Shenzhen, China, 2024, pp. 62-66, doi: 10.1109/AIEA62095.2024.10692402.
- [4] Soyeon Choi, Heehun Yang, Yunjin Noh, Giyoung Kim, Eunsang Kwon and Hoyoung Yoo, (2024) "FPGA-Based Multi-Channel Real-Time Data Acquisition System" in *Electronics*, vol. 13, no. 15, pp. 1-13, doi : 10.3390 / electronics 13152950.
- [5] Dhanabalan, G., Murugan, T. (2021). FPGA Design of SAR Type ADC Based Analog Input Module for Industrial Applications. In: Patel, Z., Gupta, S., Kumar Y. B., N. (eds) *Advances in VLSI and Embedded Systems. Lecture Notes in Electrical Engineering*, vol 676. Springer, Singapore. https://doi.org/10.1007/978-981-15-6229-7_8
- [6] Anchal Govil, Anmol Karnwal, Govinda Sindhu, Ayush Singh, and Shubham Shukla, (2022) "Design and Implementation of UART Using FPGA Board," in *International Journal for Research in Applied Science & Engineering Technology*, vol. 10, no. IV, pp. 1187-1190, doi: 10.22214/ijraset.2022.41478
- [7] Changqing Yang, Dawei Zhou and Li Lu, (2022) "Multi-channel High-speed Data Acquisition System Based on Improved SPI Communication," in *Journal of Physics: Conference Series*, vol. 2404, 2nd International Conference on Electrical Engineering and Computer Technology (ICEECT 2022), Suzhou, China, 23-25 September 2022, article 012028, doi: 10.1088/1742-6596/2404/1/012028
- [8] C. Liu and Y. Wang, "A 128-channel, 710 M samples / second, and less than 10 ps RMS resolution time-to-digital converter implemented in a Kintex-7 FPGA", *IEEE Trans. Nucl. Sci.*, vol. 62, no. 3, pp. 773783, Jun. 2015.
- [9] F. Caponio, A. Abba, N. Lusardi, and A. Geraci, "A high-precision wave union TDC implementation in FPGA", in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov. 2013, pp. 14.

- [10] E. Venialgo, N. Lusardi, F. Garzetti, A. Geraci, S. E. Brunner, D. R. Schaart, and E. Charbon, "Toward a full-flexible and fast-prototyping TOF-PET block detector based on TDC-on-FPGA," *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 3, no. 5, pp. 538–548, Sep. 2019
- [11] Lusardi, F. Garzetti, and A. Geraci, "Digital instrument with configurable hardware and firmware for multi-channel time measures," *Rev. Sci. Instrum.*, vol. 90, no. 5, May 2019, Art. no. 055113, doi: 10.1063/1.5028131.
- [12] N. Lusardi, F. Garzetti, N. Corna, R. D. Marco, and A. Geraci, "Very high-performance 24-channels time-to-digital converter in Xilinx 20-nm kintex UltraScale FPGA," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Oct. 2019, pp. 1–4.
- [13] F. Garzetti, N. Lusardi, and A. Geraci, "All-digital fully-configurable instrument for multi-channel time measurements at high performance," in *Proc. IEEE Nucl. Sci. Symp. Med. Imag. Conf. (NSS/MIC)*, Nov.2018, pp1–5.