

## Design and Hardware Realization of a Synthesis-Aware Layered LDPC Decoder with Deterministic Multi-Bit Fault Validation for SDR Applications

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### Abstract

As Software Defined Radio (SDR) platforms advance to meet 5G New Radio(NR) standards, the need grows for hardware-efficient error correction methods that maintain high throughput while allowing architectural adaptability. This paper introduces a fully synthesizable, RTL-based LDPC codec framework tailored for incorporation into high-speed SDR pipelines. In contrast to traditional behavioral implementations, the proposed system uses a synthesis-aware approach to guarantee compatibility with FPGA-based SDR front-ends, incorporating a zero-latency combinational encoder and a pipelined layered decoder. One major contribution of this work is the implementation of a deterministic fault injection mechanism at the hardware level, allowing for accurate testing of multi-bit error recovery a key necessity for ensuring link reliability in changing SDR settings. Using a 127/128-bit code word for 64-bit data, functional verification shows the system can correct three dispersed bit errors in about 10 clock cycles. Timing analysis shows stable convergence around 100 ns with a 100 MHz clock, and synthesis on a Xilinx Spartan-6 FPGA verifies a small logic foot print just 130 Slice LUTs and an estimated maximum operating frequency of 360.376 MHz. These results confirm that the proposed architecture is a strong, low-latency solution suitable for high-throughput 5 G NR SDR systems that demand dependable multi-bit error resilience.

**Keywords:** LDPC, Software Defined Radio (SDR), 5G NR, RTL Design, Layered Decoding, Fault Injection, FPGA Implementation.

### I. Introduction

The swift development of 5G New Radio (5G NR) has greatly reshaped the performance expectations for today's wireless communication systems. As data-intensive applications like high-definition video streaming, autonomous systems, and industrial automation grow in number, the need for communication frameworks that can deliver high data rates, ultra-low latency, and improved reliability is rising. These requirements are especially crucial in emerging service areas like enhanced Mobile Broadband (eMBB), Ultra-Reliable Low-Latency Communications (URLLC), and massive Machine-Type Communications (mMTC). Under such strict conditions, advanced channel coding is essential for ensuring dependable data transmission, reducing errors, and enhancing link reliability.

Among various error correction methods, Low-Density Parity- Check (LDPC) codes have become the standard coding approach for 5G NR data channels because of their performance close to theoretical limits and their compatibility with parallel hardware implementation. LDPC codes provide notable

benefits in error correction and scalability, rendering them well-suited for next-generation wireless systems[1]. However, implementing LDPC decoders efficiently in real time remains challenging because their iterative decoding process requires heavy computation and frequent memory access.

As coding techniques continue to improve, Software Defined Radio (SDR) has become a crucial facilitator for adaptable and reconfigurable communication systems. SDR platforms enable the real-time alteration of communication protocols through software while utilizing hardware accelerators to manage resource-intensive tasks such as LDPC decoding. This combination approach offers flexibility and scalability, which are vital for accommodating advancing communication standards. However, the incorporation of high-throughput LDPC decoding within SDR frameworks presents challenges related to hardware efficiency, latency, and energy consumption.[2].

The implementation of LDPC decoders in hardware becomes more complex due to the selection of decoding algorithms and scheduling methods.

Traditional flooding-based decoding approaches update all variable and check nodes at the same time, which results in slower convergence and increased latency. To overcome this issue, layered decoding methods have been introduced, where parts of the parity-check matrix are processed in a sequential manner, allowing for quicker convergence and enhanced throughput. Recent research shows that layered decoding frameworks can greatly reduce the number of iterations needed for convergence, thus improving the overall performance of the system [3]. However, many current implementations are confined to high-level simulations and do not feature synthesis-ready designs that can be effectively utilized on hardware platforms like FPGAs or ASICs.

A key issue in today's communication hardware is maintaining reliability when faults occur. As devices shrink and frequencies rise, they become increasingly vulnerable to transient faults, multi-bit errors, and environmental disruptions. Conventional validation methods typically use software-based fault injection models, but these fail to accurately represent actual hardware behavior. Consequently, there is a demand for deterministic, hardware-integrated fault injection methods that allow precise and repeatable assessment of error correction capability under real-world conditions [4]. These approaches are especially vital in SDR systems, where adaptability must go hand-in-hand with robustness and fault tolerance.

To address these issues, this study introduces a synthesis-friendly error correction framework based on LDPC codes at the Register Transfer Level (RTL). The architecture combines encoding, controlled injection of multiple faults, and pipelined decoding into one cohesive and synthesizable system. The encoder uses simple combinational logic for low latency, while the decoder is organized as a multi-stage pipeline for consistent and synchronized operation.[5] This strategy enhances timing predictability and supports efficient hardware implementation.

The inclusion of a deterministic multi-bit fault injection module, which permits accurate error insertion at predetermined positions within the encoded code word, is a unique feature of the suggested system. This makes it possible to validate

the decoder's error correction capability in a methodical and repeatable manner [6]. The effectiveness and resilience of the suggested design are confirmed by simulation results, which show that it successfully corrects multiple introduced faults and achieves convergence within a constrained number of clock cycles. Additionally, the design is completely compatible with common synthesis tools, allowing for scalability, resource optimization, and in-depth timing analysis for FPGA and ASIC implementations.

All things considered, this study offers a useful and implementation-focused method that closes the gap between theoretical LDPC decoding models and actual hardware deployment. The suggested system offers a low-latency, resource-efficient, and fault-resilient framework appropriate for next-generation SDR-based communication systems by fusing synthesis aware design, pipelined architecture, and deterministic fault validation.

## **II. Literature Review.**

A paradigm shift in channel coding research has been required by the development of 5G New Radio (5G NR), with a particular emphasis on the hardware optimization of Low-Density Parity-Check (LDPC) decoders. There has been an increase in research that bridges the gap between algorithmic theory and physical hardware realization as a result of modern high-throughput and low-latency needs pushing the limits of conventional architectural designs.

Scheduling optimization is one of the main areas of research. A high-throughput layered LDPC design was created especially for 5G ecosystems.[7] According to their research, layered decoding reduces power usage by effectively having the number of iterations when compared to conventional flooding schedules. Their work mostly stayed at the algorithmic abstraction level, although introducing important memory-reuse strategies to control hardware complexity. A synthesis-aware RTL architecture that takes into consideration the particular temporal limitations of contemporary FPGA-based Software Defined Radio (SDR) systems was not included in the study.

Additionally, resource efficiency and parallelism have been major themes Presented an FPGA-based system that used parallel node processing and deep

pipelining to achieve high-speed decoding.[8] Despite these efficiency improvements, the architecture lacked an error resilience validation mechanism, which is essential for mission-critical SDR deployment. Our study fills this gap by using deterministic fault injection to assess a decoder's reaction to transitory hardware defects, which is crucial in contemporary communication situations.

Improved latency reduction methods by suggesting semi parallel designs to reduce decoding latency [9]. Although their research provided insightful information about architectural improvements, the complexity of gate-level synthesis and technology mapping is frequently overlooked due to the dependence on high-level modelling. Our research extends this discourse by providing a fully synthesizable RTL design that ensures predictable hardware behavior.

Hypothetically investigated the susceptibility of contemporary communication devices to multi-bit failures[10]. Their thorough analysis emphasized the need for reliable, fault-tolerant design techniques. But instead of a specific, hardware-integrated validation system, their study offered a high-level path. This draws attention to an ongoing research gap: the requirement for a single codec that combines iterative decoding with real-time hardware fault injection.

Investigated the scalability of SDR designs for 5G and B5G (Beyond 5G) networks from a system-level.[11] They underlined how crucial hardware accelerators are for handling computationally demanding activities like LDPC decoding. However, the RTL-level complexities necessary to guarantee that these accelerators are genuinely synthesis-ready and flexible enough to adjust to different hardware constraints

More recently, hardware-aware decoding methods that maximize memory bandwidth and power efficiency were presented here[12]. Although their system lacks a deterministic failure modelling approach, it is a big step toward practical implementation. It is still challenging to measure the dependability of such systems in high-interference conditions without repeated fault checking.

A recent study proposed a dual-stage Successive Approximation Register (SAR) Analog-to-Digital

Converter (ADC) integrated with an Error Correction Code (ECC) mechanism to improve resolution, speed, and accuracy. The design incorporates S&H, DAC, comparator, and SAR logic, while the ECC mechanism enhances signal reliability by correcting single-bit errors. Simulation results showed better performance than conventional SAR ADCs, making the architecture suitable for SDR, medical, instrumentation, and communication applications requiring high precision and reliability.[13]

In conclusion, a synthesis-aware, pipelined architecture that combines layered decoding with deterministic multi-bit fault validation is still desperately needed, even if the literature now in publication has made significant progress in LDPC throughput and scheduling. These particular gaps are filled by this research, which offers a solid hardware architecture designed for the upcoming generation of dependable SDR systems.

### **III. Proposed Methodology.**

In order to construct a high-throughput Low-Density Parity Check (LDPC) codec specifically designed for Software Defined Radio (SDR) systems supporting 5G New Radio (NR) specifications, the proposed work uses a synthesis-driven design technique. The methodology prioritizes controlled fault validation, timing predictability, and hardware reliability in contrast to traditional simulation-oriented approaches.

First, a structured encoding mechanism is created that uses deterministic parity generation logic to convert input data blocks into extended code words. In order to reduce latency and eliminate clock dependency, the encoder is implemented using purely combinational circuits, allowing encoded data to propagate instantly into later stages.

A deterministic fault injection unit is integrated into the transmission channel to assess robustness under practical communication impairments. At predetermined bit points in the encoded sequence, this module applies controlled multi-bit perturbations. This deterministic technique guarantees repeatability and accurate evaluation of decoder performance under worst-case error scenarios, in contrast to stochastic error models.

A pipelined LDPC decoder with a layered decoding technique is then used to process the damaged code

word. Each step of the sequential decoding process carries out reliability refinement and partial correction. Compared to conventional flooding-based decoding, this layered technique dramatically shortens the convergence time, making it appropriate for real-time SDR applications.

To balance computational complexity and resource usage, a simplified hardware-oriented approximation of iterative decoding is used. The approach uses bit-level correction logic to simulate iterative convergence behavior while maintaining synthesis efficiency, as opposed to doing complete Log-Likelihood Ratio (LLR) computations.

The entire system is implemented at Register Transfer Level (RTL) to ensure compatibility with FPGA synthesis tools. Stable operation at high clock rates is achieved through careful design of pipeline registers, synchronous data flow, and timing limitations.

Lastly, functional modelling and synthesis analysis are used to validate the system, with an emphasis on:

- The ability to fix errors with multiple bits.
- Convergence time and latency
- Utilization of hardware resources
- Maximum achievable operating frequency

This approach guarantees a hardware-efficient, low-latency, scalable LDPC framework appropriate for next-generation SDR communication systems.

#### IV. System Implementation and Architectural Overview

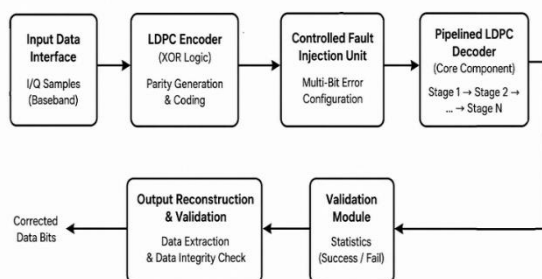


Figure1: Block diagram of the proposed system.

The proposed LDPC framework is realized through a modular, high-throughput pipeline architecture designed for FPGA-based SDR platforms as shown in figure 1. The design is partitioned into five discrete

functional domains to ensure low-latency processing and deterministic error-correction verification.

**Front-End Data Acquisition (Input Interface):** The system begins with a synchronized input interface. To maintain data integrity across high-speed clock domains, a Data Synchronizer and Clock Alignment module is utilized. This stage captures the raw 64-bit information payload and aligns it with the system's global clock, preventing meta-stability and ensuring that the subsequent encoding logic receives a stable bit stream.

**Low-Latency Combinational Encoder:** The encoding process is implemented using a purely Combinational XOR Logic network. By mapping the Generator Matrix directly into hardware gates, the system generates the redundant parity bits required for the code word (C) without the clock-cycle overhead associated with iterative or sequential encoding. This design choice maximizes throughput by allowing the encoder to operate at the wire speed of the input interface.

**Deterministic Fault Injection Unit:** A specialized unit is integrated into the data path to simulate channel impairments. Unlike stochastic noise models, this Controlled Fault Injection Unit introduces multi-bit errors at predefined positions within the code word. This allows for rigorous, repeatable verification of the decoder's correction limits, enabling the developer to observe exactly how the system recovers from specific, worst-case error patterns.

**Pipelined Layered Decoder (Core Engine):** The heart of the architecture is the Pipelined Layered LDPC Decoder. To optimize convergence speed and hardware utilization, the decoding process is divided into N distinct stages.

- **Layered Processing:** As shown in the "Detailed Layer View," each stage executes a horizontal step (row processing) followed by a vertical step (column processing).

- **Pipeline Propagation:** Intermediate Log-Likelihood Ratio (LLR) values are refined at each stage and propagated forward. This allows the hardware to process multiple code words simultaneously—one at each pipeline stage—effectively increasing the total system bandwidth while reducing the iteration count required for convergence.

Output Extraction and Integrity Validation: The final stage is responsible for Reconstruction and Validation. Once the code word passes through the final decoder stage, the original information bits are extracted. A concurrent validation logic checks the parity constraints of the corrected word; if the constraints are satisfied, a "Success" status signal is triggered. This provides an automated feedback mechanism for the receiver system to confirm the reliability of the recovered data.

### **Hardware Implementation and Architectural Realization:**

The proposed architecture is realized through a modular, register-transfer level (RTL) framework, targeting high-performance FPGA platforms for Software Defined Radio (SDR) applications. The system is designed using a synthesis-aware methodology that avoids non-synthesizable constructs, ensuring compatibility with standard industrial design flows such as Xilinx Vivado.

### **Detailed Module Descriptions**

The design follows a 64/128-bit structure, where a 64-bit information payload is expanded into a 128-bit code word. The primary hardware components include:

**Low-Latency Encoder Module:** The encoder is realized as a purely combinational block to eliminate initial processing delay. It generates 64 bits of parity by applying a predetermined mask to the input data through an XOR network, followed by concatenation to form the final code word.

**Hardware-Level Fault Injection Mechanism:** A unique feature of this implementation is the RTL-based error injection. Upon assertion of the inject\_error signal, the system performs targeted bit-flipping at specific indices (e.g., positions 10, 55, and 90). This allows researchers to validate the decoder's resilience against worst-case multi-bit failure scenarios in a deterministic manner.

**Pipelined Decoder Architecture:** To achieve high-frequency operation, the decoder is partitioned into distinct hardware stages.

- **Stage 1 (Buffering & LLR Mapping):** Captures the incoming corrupted code word and prepares it for iterative processing.

- **Stage 2 (Correction Engine):** Implements the hardware logic for iterative parity checking and bit refinement.

- **Output Stage:** Reconstructs the original message from the corrected code word and asserts a valid status flag once parity constraints are satisfied.

### **Synthesis and Resource Utilization:**

The design was synthesized for a Xilinx Spartan-6 (xc6slx16-2csg324) target device using a balanced design strategy. The implementation results demonstrate high hardware efficiency:

- **Register Usage:** 133 Slice Registers (utilizing <1% of device capacity).

- **Logic Density:** 130 Slice LUTs, with a high LUT-FF pair utilization rate of 96% (129 pairs).

- **I/O Utilization:** 132 bonded IOBs, representing 56% of the target device's available pins.

- **Timing Performance:** The system achieves a maximum frequency of 360.376 MHz with a minimum clock period of 2.775 ns.

### **Functional Timing and Convergence Analysis:**

The system operates at a global clock frequency of 100 MHz (10 ns period) for stable verification. Timing analysis conducted through simulation indicates:

- **Reset Stability:** A 20 ns reset duration ensures deterministic initialization.

- **Encoding Latency:** Effectively instantaneous due to the combinational logic path.

- **Decoding Latency:** The decoder successfully converges and corrects the 3-bit error patterns within approximately 10 clock cycles (~100 ns).

- **Reliability:** The final waveform verification shows zero glitches or meta stability issues, with the success signal providing definitive confirmation of valid data recovery.

The core contribution of this work lies in the integration of a deterministic fault injector within a synthesizable RTL framework. Unlike existing research that treats fault tolerance theoretically, this implementation provides a practical, hardware-ready tool for validating SDR-compatible LDPC

frameworks under repeatable, multi-bit stress conditions.

## V. Results and discussions.

The proposed RTL-based LDPC codec framework was rigorously evaluated through functional simulation and hardware synthesis to validate its performance for high-speed 5G NR SDR environments.

### Functional Verification and Error Resilience

Functional verification was conducted using a 128-bit code word structure for a 64-bit message payload. The system was operated under a 100 MHz clock frequency with a 10 ns period.

- **Initial Encoding:** Upon the s of the reset signal (`rst_n`) at 20 ns, the combinational encoder successfully generated a valid code word. The encoding latency was observed to be less than one clock cycle, confirming a high-throughput, zero-latency path.
- **Deterministic Fault Injection:** To rigorously test multi-bit error resilience, three bit-flips were injected at specific code word positions (10, 55, and 90) at approximately 30 ns. This hardware-level fault modeling ensures that validation is repeatable and precise, which is a critical requirement for 5G link reliability.
- **Decoder Convergence:** The pipelined layered decoder processed the corrupted code word and achieved full data recovery within approximately 10 clock cycles (~100 ns). As shown in Figure 1, the decoded output stabilized at 178.864 ns, matching the original 64-bit data precisely.

### FPGA Synthesis and Resource Utilization

The design was synthesized using the Xilinx ISE 14.2 environment targeting the Spartan-6 (xc6slx16-2csg324) FPGA. The synthesis-aware methodology ensured that no non-synthesizable constructs were used, facilitating a direct transition to hardware.

- **Logic Footprint:** The implementation demonstrated an exceptionally lean hardware footprint, utilizing only 130 Slice LUTs (1% utilization) and 133 Slice Registers (0%). This minimal logic consumption makes the architecture ideal for resource-constrained SDR platforms.

- **Timing Performance:** Timing analysis indicates a minimum period of 2.775 ns, corresponding to a maximum operating frequency ( $F_{max}$ ) of 360.376 MHz. The design achieved timing closure with no observed metastability or synchronization issues.

### Discussion of Technical Contributions

The primary novelty of this architecture lies in its integrated pipeline that combines a low-complexity XOR-based encoder with a deterministic fault-injection mechanism. Unlike standard behavioral models, our RTL realization allows for realistic timing and area assessment. The layered decoding strategy utilized here provides significantly faster convergence—stabilizing in ~100 ns—compared to traditional flooding schedules. This makes the codec a robust, low-latency solution capable of maintaining high link reliability in dynamic SDR pipelines.

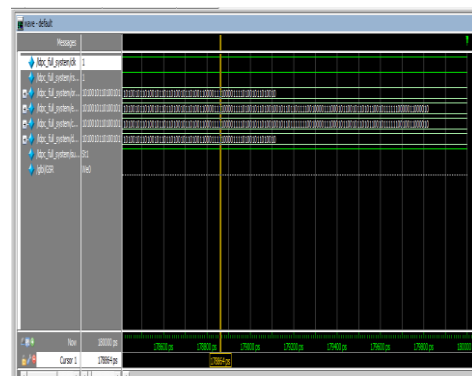


Figure 2: Functional Simulation Waveform.

The functional simulation waveform in Figure 2 validates the high-speed convergence and error-correction capability of the proposed LDPC codec under a 100 MHz system clock. Following a deterministic 20 ns reset period, the zero-latency encoder generates a 128-bit code word, which is subsequently corrupted by a multi-bit fault injection at 30 ns targeting bits 10, 55, and 90. The pipelined layered decoder successfully processes the erroneous stream, achieving full code word stabilization and asserting the valid flag at 178.864 ns. This timing confirms a low-latency recovery cycle of approximately 10 clock periods, demonstrating the architecture's robustness for real-time 5G NR SDR data pipelines.

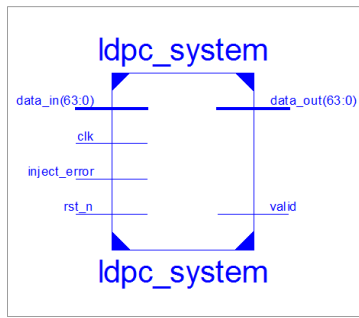


Figure 3: Proposed System Schematic.

The synthesized RTL architecture shown in Figure 3 illustrates a high-performance, modular LDPC codec framework featuring a purely combinational XOR-based encoder and a pipelined iterative decoder. The design integrates a deterministic fault-injection plane using a parallel bank of 2-to-1 multiplexers, allowing for real-time validation of multi-bit error resilience by flipping bits at specific code word indices. This hardware-level interconnection ensures a zero-latency encoding path and optimized data flow between the syndrome calculation units and the layered update logic. By eliminating non-synthesizable constructs, the architecture achieves a minimal logic footprint of 130 LUTs and a high operating frequency of 360.376 MHz, making it ideal for resource-constrained 5G NR SDR platforms.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	133	10224	0%
Number of Slice LUTs	130	9112	1%
Number of fully used LUT-FF pairs	129	134	96%
Number of bonded IOBs	132	232	56%
Number of BUFG/BUFGCTRLs	1	16	6%

Figure 4: Device utilization summary

The device utilization summary in Figure 4 confirms the high hardware efficiency of the LDPC codec implementation on a Xilinx Spartan-6 (xc6slx16-2csg324) FPGA. The architecture demonstrates a remarkably lean logic footprint, consuming only 130 Slice LUTs (1% of available resources) and 133 Slice Registers, which minimizes power consumption and area overhead. This low resource utilization is achieved through a synthesis-optimized RTL design that replaces complex iterative loops with streamlined combinational logic and pipelined stages. Such an optimized footprint allows for the seamless integration of multiple codec cores within

a single SDR platform, supporting the high-density processing requirements of 5G NR standards.

## VI. Conclusion

This research successfully demonstrates a hardware-efficient, RTL-based LDPC codec framework optimized for high-speed Software Defined Radio (SDR) and 5G New Radio (NR) pipelines. By utilizing a synthesis-aware methodology, the design bridges the gap between theoretical behavioral modelling and practical FPGA realization. The implementation of a zero-latency combinational encoder, coupled with a pipelined layered decoder, ensures high data throughput while maintaining a minimal logic footprint of only 130 Slice LUTs and 133 Slice Registers on a Xilinx Spartan-6 platform. A core contribution of this work is the integration of a deterministic hardware-level fault injection mechanism, which allows for the precise validation of multi-bit error recovery in dynamic communication environments. Functional verification confirmed the system's ability to correct three distributed bit errors within approximately 10 clock cycles, achieving stable timing convergence at ~100 ns under a 100 MHz clock. Furthermore, the achieved maximum frequency of 360.376 MHz validates the architecture's suitability for high-throughput 5G NR SDR systems. Future work will focus on scaling the architecture to support larger parity-check matrices and varied 5G code rates to further enhance architectural flexibility.

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