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Enhanced Quantum FTRA with Integrated Fault Masking, Detection and Localization Mechanism

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Abstract

Quantum circuits are susceptible to errors and building a fault tolerant reliable quantum circuit is critical. This paper proposes a hybrid Quantum Fault Tolerant Reversible Adder/Subtractor with fault masking, detecting and locating mechanism. The presented hybrid reversible gate design with parity preserving reversible gates that enabled better circuit robustness was implemented using IBM Quantum Composer. To overcome the faults and enhance overall circuit robustness a Triple Modular Redundancy (TMR) based approach is integrated with the 3-bit majority voter circuit. Additionally, fault detection and locating mechanisms are also used to detect the fault occurrence. Simulation studies for the presented quantum circuit design was also verified using IBM Quantum Simulator. The results obtained confirmed that the combination of fault masking, detection and locating mechanisms improved the overall performance and reliability of the quantum circuit. The overall framework proposed provides a practical model for the development of a fault tolerant reversible logical circuits for various quantum applications.

Keywords - Quantum computing, fault tolerance, reversible circuits, quantum circuits, qubits, fault masking, locating mechanism.

Introduction

Quantum computing uses the laws of quantum mechanics to perform operations on data. Devices that perform quantum computations are known as Quantum Computers which are considered to be the next generation of computers. Even though the quantum processor is smaller and consumes less energy than existing supercomputers, the quantum hardware appears to be large, consisting primarily of cooling mechanisms to keep the superconducting processor at its ultra-low operating temperature. Since Quantum Computers operate on qubits, they are highly prone to errors. When a qubit interacts with its surroundings, it exhibits decoherence, which results in disruptions and collapse superposition leading to errors in quantum computational systems. Hence it is essential to build a fault-tolerant quantum circuit since they continue to operate as intended even in the presence of faults.

A digital combinational logic circuit is said to be reversible based on its ability to convert any given input pattern into a unique output pattern. Reversible circuits are popular in the field of nanotechnology, optical computing, quantum computing, and low-power CMOS design. Though reversible circuits provide structural compatibility but are not sufficient enough for a quantum hardware under a noisy environment. Hence, reversible logic is combined with fault tolerance mechanism for improving performance of quantum circuits. Fault Tolerant reversible Architectures incorporate fault masking, detection and localization mechanisms thereby achieving quantum circuit reliability. Quantum fault tolerant schemes have to operate based on quantum coherence unlike classical design. These constraints result in the use of reversible and controlled gates to detect and suppress the effects of faults without qubit loss.

This paper proposes a quantum FTRA including Fault Masking, Detecting and Locating Mechanism using IBM quantum composer. The proposed architecture consists of an adder and subtractor module integrated with fault tolerant mechanisms.

Literature Review

A quantum gate is an elementary unit of quantum circuit that performs operations on qubits like classical logic gates in a conventional digital circuit

that operates on binary digits. Due to the reversibility of quantum gates, which result in a distinct output y for each input x, it is possible to exclusively recover the inputs of reversible gates from their outputs, preventing data loss and lowering power consumption. **Matthew Kiser et al (2024)** presented a quantum-enhanced auxiliary field quantum Monte Carlo (QC-AFQMC) that investigates classical and quantum costs associated with measurement strategies required for estimating overlaps between walker states and trial wave functions prepared on quantum devices [1]. **Rakshith Saligram et al. (2013)** claimed that their proposed methodologies are fault-tolerant after assuring parity-preservation in their reversible circuit designs [2]. Parity-preservation is preferred for testing if a circuit's output is right or erroneous. A fault-tolerant circuit, on the other hand, must be able to give a corrected output even when the circuit is faulty. Because parity preservation is only used to detect fault, it does not guarantee fault tolerance. As a result, parity-preserving logic based designs cannot be classified as fault-tolerant. **Maity et al. (2019)** presented a reversible logic based optimized 2:4 decoder, the design focused on minimising quantum cost, garbage input and constant input. The proposed design used one Peres gate, one NOT gate and four Faynman gates [3]. **Ali et al. (2015)** proposed two new approaches that were used to decompose Toffoli gates using MCT-based circuits to match with respective quantum realizations [4]. **Abdessaied et al. (2013)** presented a novel optimized reversible logic circuit using Boolean satisfiability for template matching to address low power circuit design in quantum computing. It cannot be guaranteed that a matching cascade will always be found because these techniques are dependent on heuristics [5]. **Garipelly et al. (2013)** presented fundamental reversible logic gates that are applicable to develop higher-order systems that use reversible circuits as a fundamental building block and that can use quantum computers to carry out more difficult functions [6]. **Rahman et al. (2011)** provided a library containing two-qubit quantum gates that are not capable of producing entangled states. In the suggested library quantum cost per two-qubit gate is one. These gates can therefore lower the quantum costs of reversible circuits [7]. **Miller et al. (2003)** presented a transformation-based algorithm for creating this type of a reversible circuit using n×n Toffoli gates [8]. Then, straightforward template matching was used to apply reduction rules. For 3-input circuits, the approach yields solutions that are almost ideal and it also yields excellent results for larger issues. **Maslov et al. (2005)** examined templates used to streamline a quantum circuit that was previously discovered using another method. Then, the authors provided specific information for circuits composed of NOT, CNOT and controlled-sqrt-of-NOT gates with quantum cost reduction [9]. **Thomsen et al. (2008)** proposed an improved 13×13 reversible logic circuit for a 1-decimal BCD full-adder that is quicker, more efficient and uses fewer garbage bits. With a delay of only m + 17, it can provide a rapid, low-power, reversible m-decimal BCD full-adder [10]. **Thapliyal et al. (2009)** indicated that numerous applications of reversible logic can be found in low power VLSI architecture, quantum dot cellular automata, optical computing, and quantum computing [11]. **Miller et al. (2010)** presented a line addition approach to reduce the quantum cost or the quantity of transistors in CMOS implementation. Experiments proved that the cost reductions can be substantial even with the addition of only a few lines (or even just one), provided that other circuit modifications are already in place [12]. **Szyprowski et al. (2011)** addressed quantum cost minimization in a 4-bit reversible Toffoli circuit through a tool that implemented all circuits with specified gate counts and identified the circuits with minimum quantum cost. It is demonstrated that, when compared to well-known circuits, benchmarks and designs derived from current publications can result in quantum cost savings of up to 74% [13]. **Thapliyal et al. (2011)** proposed a novel reversible half subtractor design based on the realization of the reversible TR gate via quantum gates. The 2x2 quantum gates CNOT, Controlled-V and Controlled-V^+ gates are used to create the reversible TR gate [14]. **Rangaraju et al. (2014)** presented a reversible 8-bit parallel binary adder/subtractor with designs I, II and III, which implemented complete adders and subtractors in a single unit [15].

These studies highlight the importance of a cost effective, reversible and scalable quantum circuit design. Existing literature also discusses the progress in design and implementation of reversible quantum circuits. A number of research has been carried out on parity preserving reversible logic for fault detection and also towards quantum circuit design, implementation and optimization. Despite the contributions made, realisation of fault tolerant quantum circuits still remains a challenging problem. Hence, there is a necessity to develop a fault tolerant reversible framework with fault detection and locating mechanism with reduced quantum cost. This work presents a framework with FTRA working as both adder and subtractor utilising Triple Modular Redundancy (TMR) for fault masking.

Fault-Tolerant Reversible Adder

A fault-tolerant system is one that makes the system reliable by continuing its operation correctly even in the presence of faults [15]. Parity-preserving alone does not guarantee fault tolerance. Therefore, it is crucial to build a fault-tolerant system.

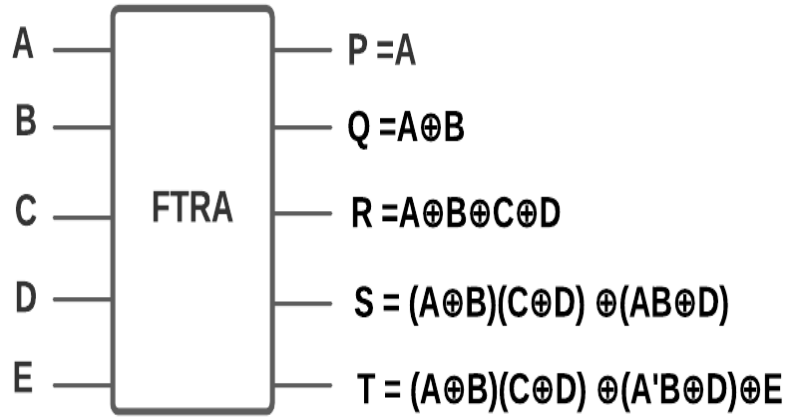

Figure 1. FTRA Gate

Fig. 1 shows Fault-Tolerant Reversible Adder (FTRA) which is a 5×5 parity-preserving reversible gate which can be synthesized to work as a full adder as well as full subtractor. Let the input vectors of FTRA be A,B,C,D,E and the output vector is considered as P,Q,R,S,T then FTRA works as full adder with three inputs A, B and Cin fed to A, B and C lines respectively D and E are made zero. Sum is obtained in R line and Cout is obtained in S line. While for subtraction, inputs A, B and Bin fed to A, B and D lines respectively C and E are made zero.

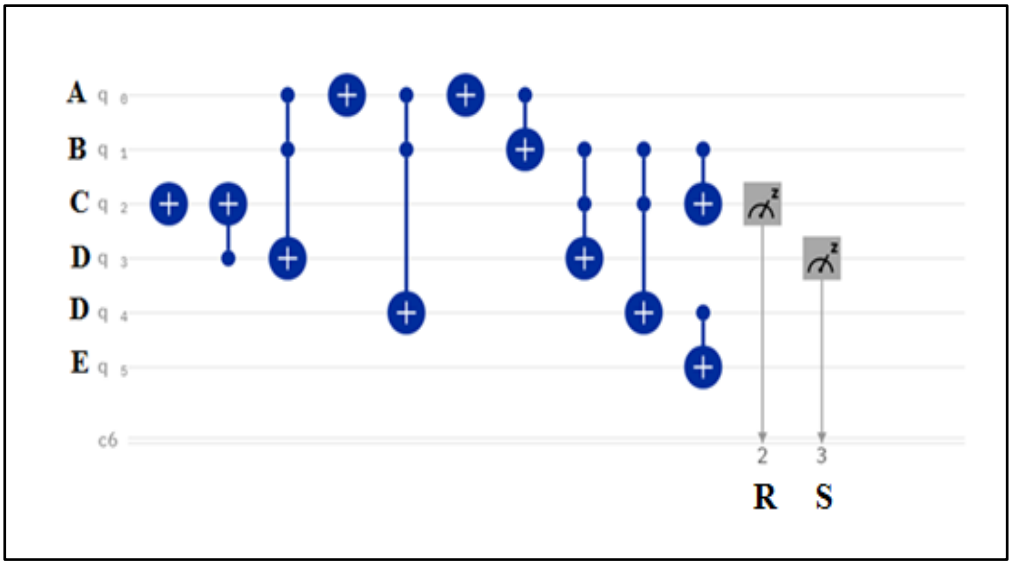

Figure 2. Quantum Realization of FTRA Gate (Adder)

Quantum realization of FTRA synthesized to work as a Full Adder represented in Fig. 2. The A, B and C inputs are fed with 001, resulting in 1 output given by the R line representing sum output and 0 output given by the S line representing carry output. The correctness of the design was verified by simulating the circuit using the IBMQ simulator.

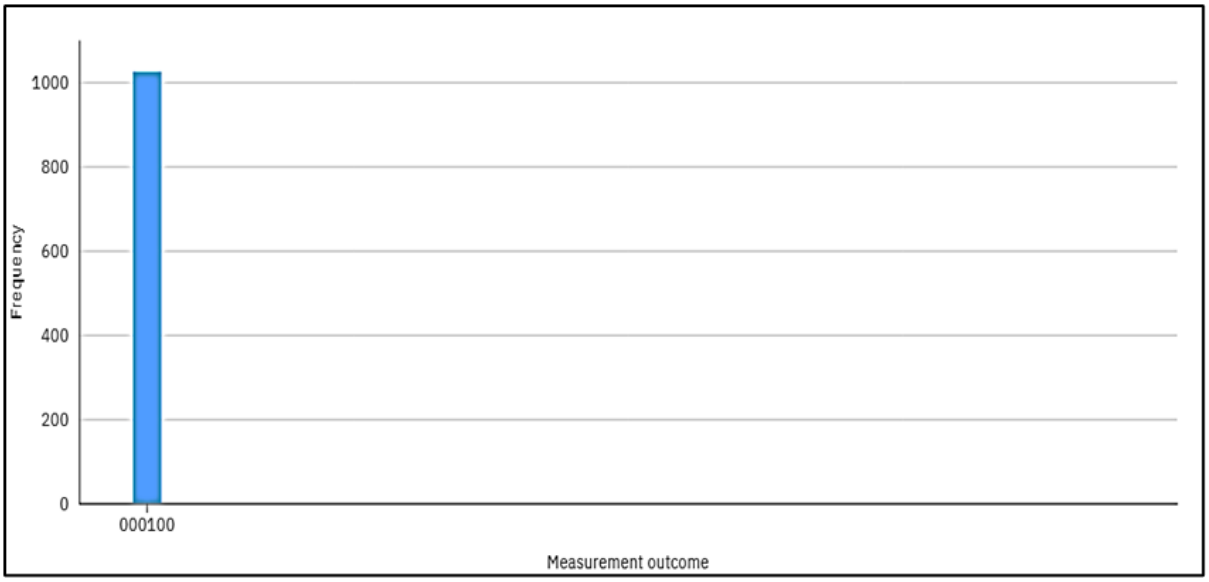

Figure 3. Output of Quantum FTRA synthesised to function as Adder

Fig. 3. shows the resultant histogram of frequency distribution with the measurement outcome of quantum FTRA as a Full adder on simulating the circuit using ibmq_qasm_simulator. The resultant obtained from $q_5q_4q_3q_2q_1q_0$ on measurement is 000100 where q_2 corresponds to sum output, q_3 corresponds to carry while the other outputs are of garbage values.

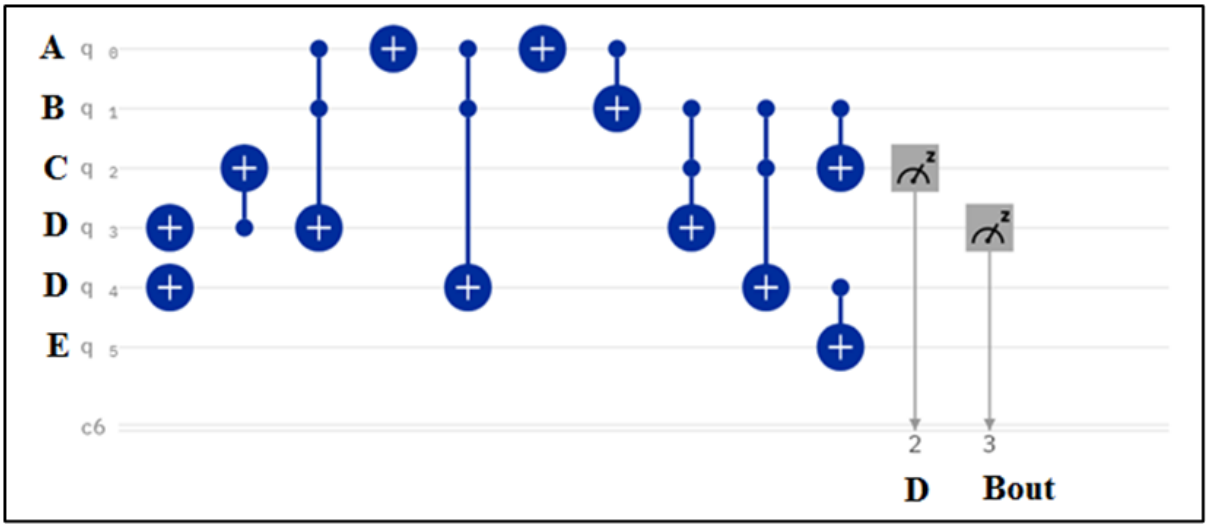

Figure 4. Quantum Realization of FTRA Gate (Subtractor)

Fig. 4. shows the FTRA quantum realization synthesized to work as a Full Subtractor. The A, B and D inputs are fed with 001, resulting in 1 output given by the R line representing difference and 1 output given by the S line representing borrow. The correctness of the design was verified by simulating the circuit using the IBMQ simulator.

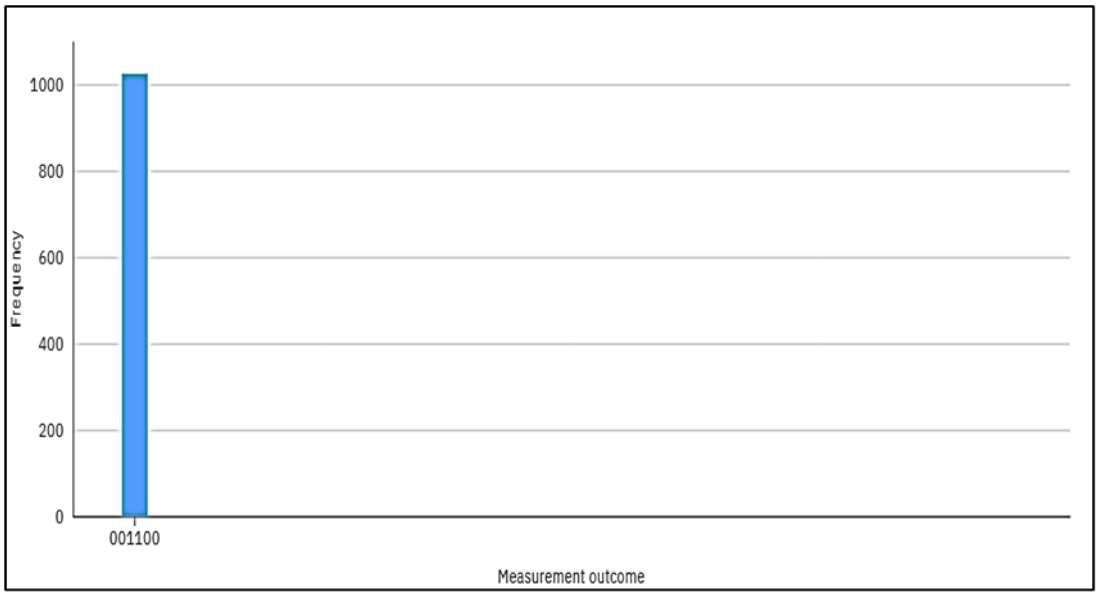

Figure 5. Output of Quantum FTRA synthesised to function as Subtractor

Fig. 5. shows the resultant histogram of frequency distribution with the measurement outcome of quantum FTRA as a Full Subtractor on simulating the circuit using ibmq_qasm_simulator. The resultant obtained from $q_5q_4q_3q_2q_1q_0$ on measurement is 001100 where q_2 corresponds to Difference output, q_3 corresponds to Borrow output while the other outputs are of garbage values.

Based on the above discussions, it can be concluded that the FTRA can be used to perform both addition and subtraction operations which is also evident from the simulation results obtained. The simulation results obtained from IBMQ simulator evaluates the correctness of the sum, carry, difference and borrow results obtained. The capability of a FTRA to perform both addition and subtraction indicates its effectiveness to be used in building quantum circuits. Arithmetic circuits are the basic block in ALU and play a key role in any computational system.

Fault Masking Technique

The frequent form of passive hardware redundancy used to create a fault-tolerant system is a triple modular redundancy (TMR) [14][15][16]. This approach involves three identical copies of the design modules and a majority voter that combines the triple module outputs. The triplicated module's majority value of the specific system is selected by the voter circuit and generates an output as shown in Fig. 6. When there is an erroneous value obtained in any one of the modules, the majority voter will be able to produce the correct results by masking them.

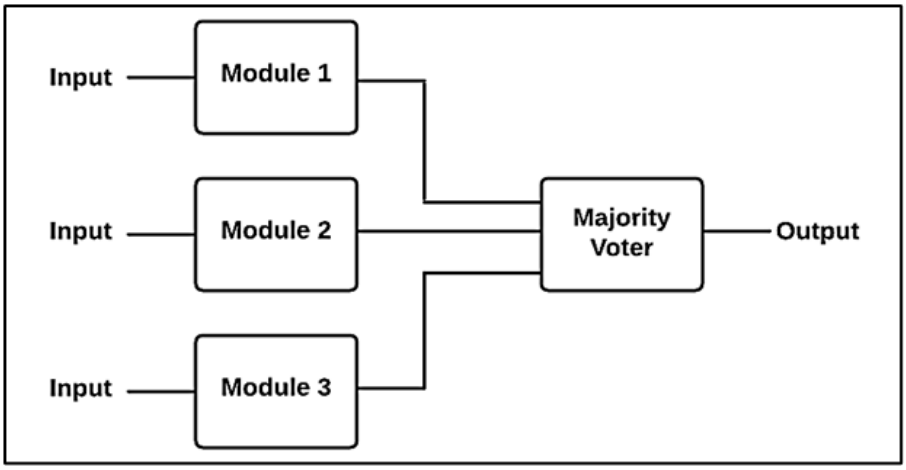

Figure 6. Fault Masking Technique

The block diagram of a 3-bit Majority voter circuit which is constructed with one Fredkin Gate and two Double Feynman Gates is represented in Fig. 7. Since the circuit consists of parity-preserving reversible gates the majority voter circuit preserves parity ensuring the testing for occurrence of faults. The quantum cost of the majority voter is 11.

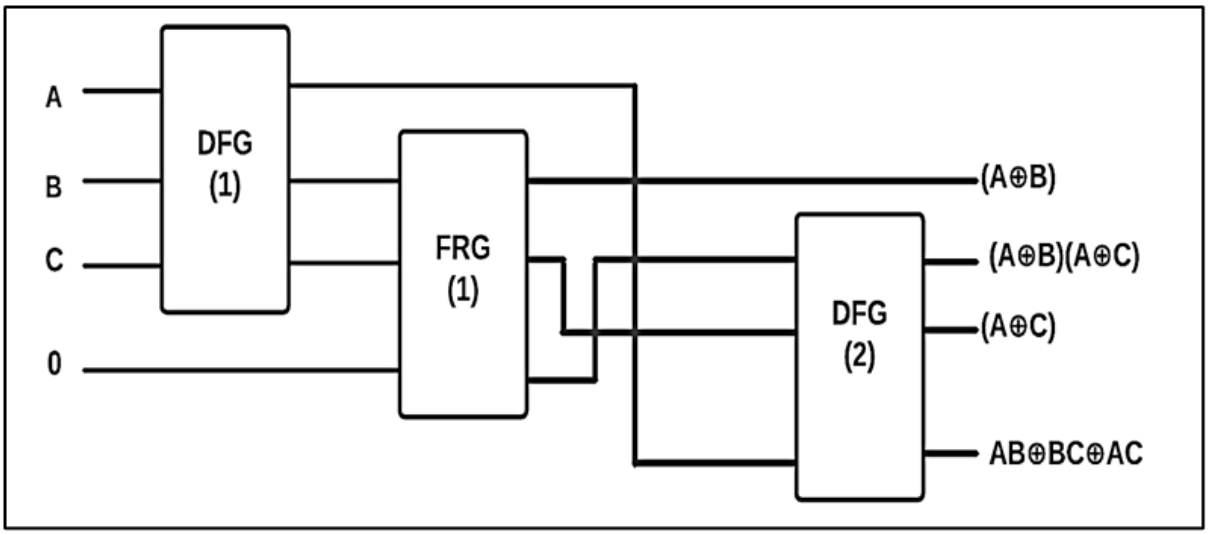

Figure 7. Block Diagram of 3-Bit Majority Voter

Fig. 8 shows the quantum realization of a 3-bit Majority Voter Circuit. The majority output among the three inputs A, B and C is given by AB⊕BC⊕AC, while the outputs A⊕B, A⊕C and (A⊕B) (A⊕C) are treated as Garbage outputs.

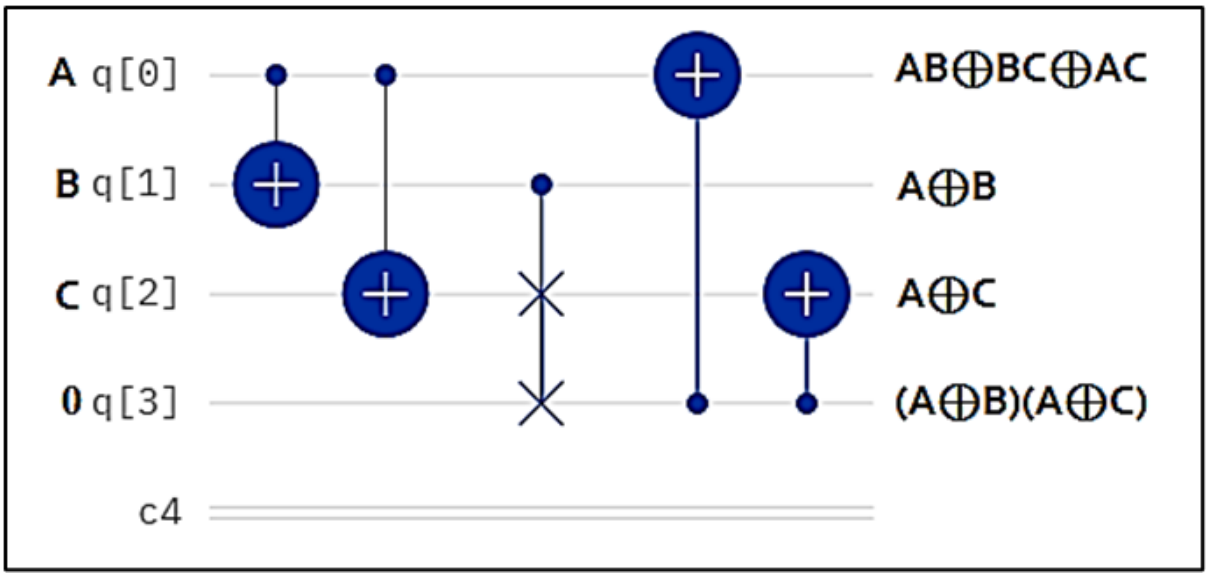

Figure 8. Quantum Realization of 3-Bit Majority Voter Circuit

The functionality of the 3-bit Majority Voter Circuit is shown in Table. 1.

Table 1. Function Table of 3-Bit Majority Voter

Inputs	**Majority Output**	**Garbage Outputs**		
ABC	**AB⊕BC⊕AC**	**A⊕B**	**A⊕C**	**(A⊕B)(A⊕C)**
000	0	0	0	0
001	0	0	1	0

010	0	1	0	0
011	1	1	1	1
100	0	1	1	1
101	1	1	0	0
110	1	0	1	0
111	1	0	0	0

The Triple Modular Redundancy (TMR) technique is employed in a quantum Fault-Tolerant Reversible Adder (FTRA) that is synthesised to function as a Full Adder and is depicted in Fig. 9.

As discussed a 3 majority voter circuit is used to mask the faulty output and generate the correct Sum output. Similarly an additional majority voter circuit is used in the same circuit to mask the faulty output and produce the correct carry output. The inputs to the first and second FTRA based Full adder modules are fed as A=0, B=0 and C=1, while the inputs to the third module are fed as A= 1, B=1 and C=1. The first and second module resulted with sum 1 and carry output 0. The sum output of the third module is 1 and carry output is 1. All the three sum lines produce high output and are fed to a majority voter circuit where it produces the final output as 1. While 2 out of 3 carry lines produce 0 as output and 1 carry line produces 1as output, when fed to a majority voter circuit it results in the majority value as 0.

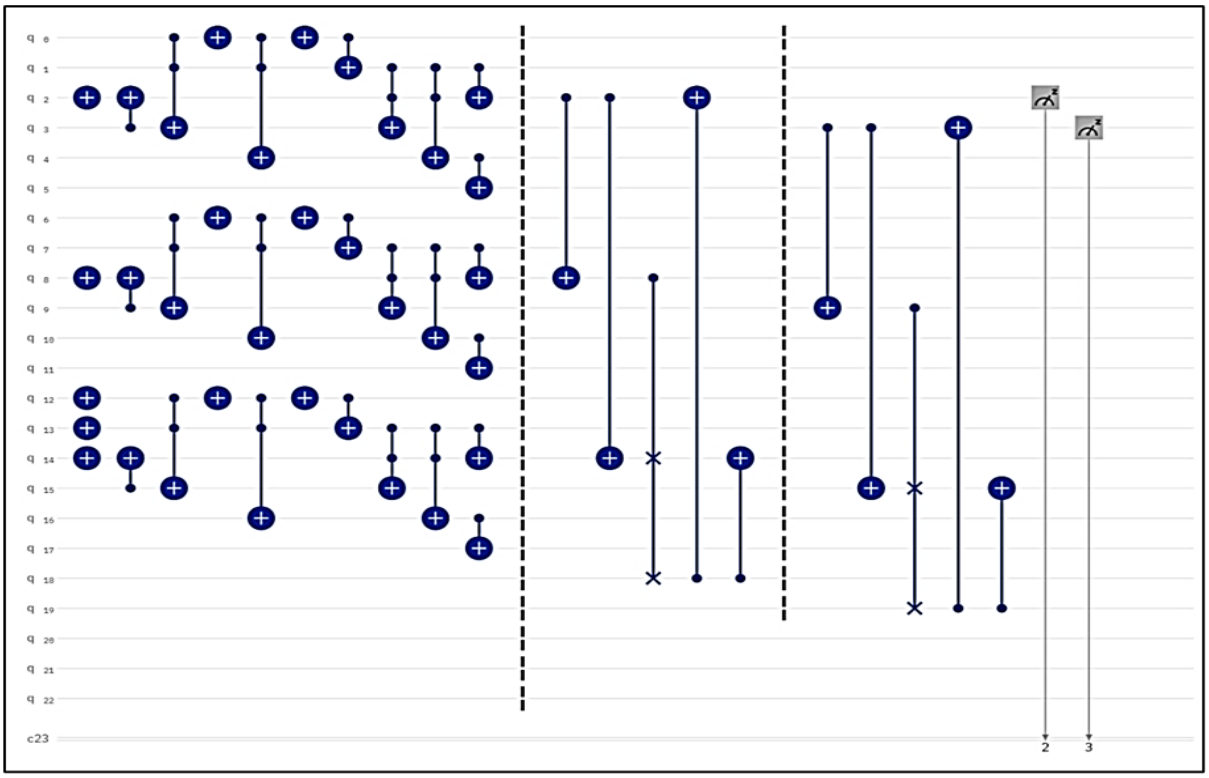

Figure 9. Quantum Fault-Tolerant Reversible Adder (FTRA) – Fault Masking

Technique (TMR)

Fault Diagnosis and Locating Technique

The quantum FTRA incorporated with the majority voter circuit shown in Fig. 10. exhibits fault masking. However, the suggested majority voter fails to diagnose and locate the single bit fault. An active technique of fault diagnosis and fault locating mechanism makes the system more reliable. Hybrid approach of achieving fault

tolerance incorporates the benefits of both active and passive techniques. Fault masking is used to prevent faults and enhanced performance is gained by incorporating fault detection and fault location mechanism.

The garbage output lines of the proposed circuit is utilized to locate the fault and additional line (A⊕B)(A⊕C)(B⊕C) is used for the diagnosis of fault. Fig. 10. shows the quantum realization of a 3-bit majority voter employed with fault diagnosis and locating mechanism that enhances system reliability.

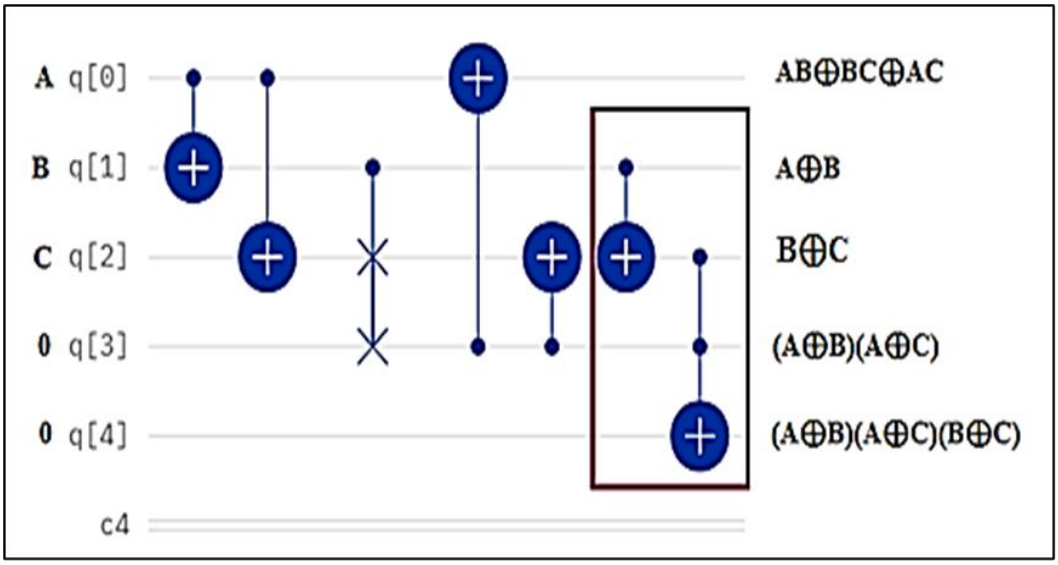

Figure 10. A 3-Bit Majority Voter including Fault Detection and Locating Mechanism

The final value of the majority voter circuits is fault free even when there are faults present. Due to which fault check line will always be zero and fault check line is one indicates faulty input lines. Now, looking at the garbage lines, if any one or more combinations of input values equal one, the circuit will have a fault. The fault is located by performing simple analysis on the garbage outputs from Table .2.

If the inputs are 001 or 110 the garbage outputs A⊕B is 0, B⊕C produces a 1 output representing input C as faulty as C is responsible for the high value produced in the garbage output B⊕C. For the inputs 010 or 101 the garbage outputs A⊕B is 1, B⊕C also produces a 1 output representing input B as faulty as B is responsible for the high value produced in the specified garbage outputs. Similarly for the inputs 011 or 100 the garbage outputs A⊕B is 1, B⊕C produces a 0 output representing input A as faulty as A is responsible for the high value produced in the garbage output A⊕B.

Table. 2. Function Table of 3-Bit Majority Voter including Fault Detection and Locating Mechanism

Inputs	**Garbage Outputs**			**Fault Check**	**Fault Location**
ABC	**A⊕B**	**B⊕C**	**(A⊕B)(A⊕C)**	**(A⊕B)(A⊕C)(B⊕C)**	
XXX	1	1	1	1	Fault in all lines
000 or 111	0	0	0	0	No Fault

001 or 110	0	1	0	0	Input C is Faulty
010 or 101	1	1	0	0	Input B is Faulty
011 or 100	1	0	1	0	Input A is Faulty

As shown in Fig. 11. a 3-bit majority voter circuit is used to mask the faulty output and generate the correct Sum output. Similarly an additional majority voter circuit is used in the same circuit to mask the faulty output and produce the correct carry output.But this kind of passive approach of fault-tolerant fails to detect and locate fault. Fig. 12. shows Quantum Fault-tolerant Reversible Adder (FTRA) which is synthesized to work as a Full Adder employed with 3-bit Majority Voter including Fault diagnosis and locating mechanism which made the design of FTRA more reliable.

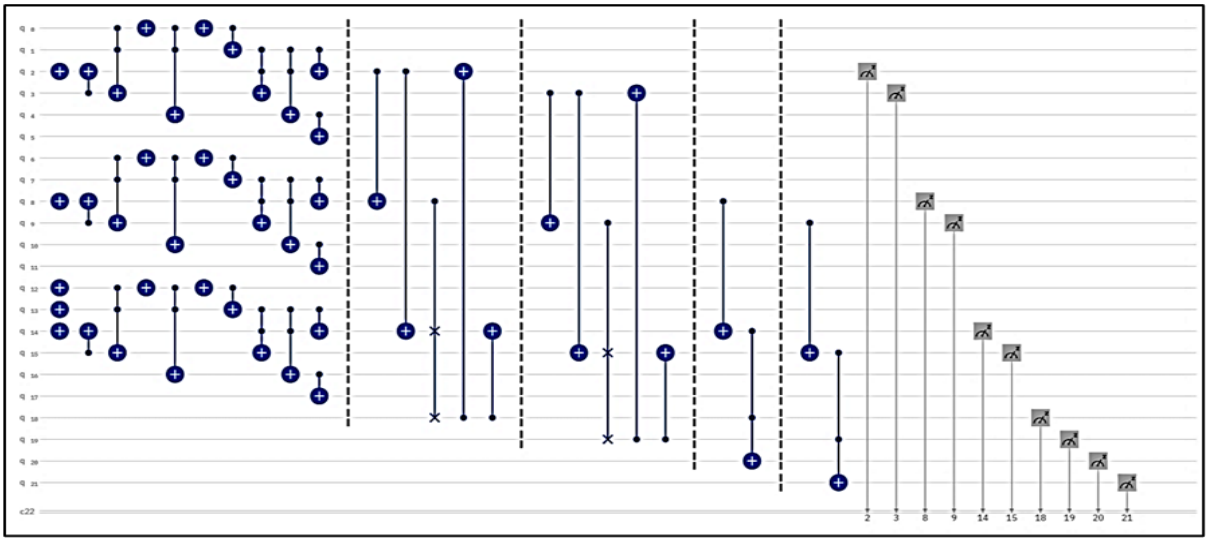

Figure 11. Quantum FTRA including Fault Masking, Detecting and Locating

Mechanism

The inputs to the first and second FTRA based Full adder modules are fed as A=0, B=0 and C=1, while the inputs to the third module are fed as A= 1, B=1 and C=1. The sum output of first and second modules is 1 and carry output is 0. The sum output of the third module is 1 and carry output is 1. All the three sum lines produce high output and are fed to a majority voter circuit where it produces the final output as 1. While 2 out of 3 carry lines produce 0 as output and 1 carry line produces 1 as output, when fed to a majority voter circuit it results in the majority value as 0. An additional circuitry is incorporated to the majority voter circuit of both Sum and Carry output of FTRA which is capable of detecting and locating the fault with respect Sum and Carry output.

The Sum output from the three modules is 111 hence according to the function table all garbage outputs produce 0 output representing that there is no occurrence of fault.While the carry output from the three modules is 001 thereby the garbage output B⊕C produces high value as output indicating that the fault is with the carry output of third module (Input C is faulty).While the fault check line of both Sum and Carry is zero indicating that all the sum and carry output lines are not faulty.

Results and Discussion

The proposed quantum FTRA employing Triple Modular Redundancy (TMR) is simulated using IBMQ simulator. The measurement outcome of the proposed design is depicted in Fig. 12. as 0x4, which represents the values 00000000000000000000100, where the third bit from the right corresponds to the sum output and the fourth bit from the right corresponds to carry output, which is the majority output among three output values. As a result, a valid output is generated while the faulty output is masked.

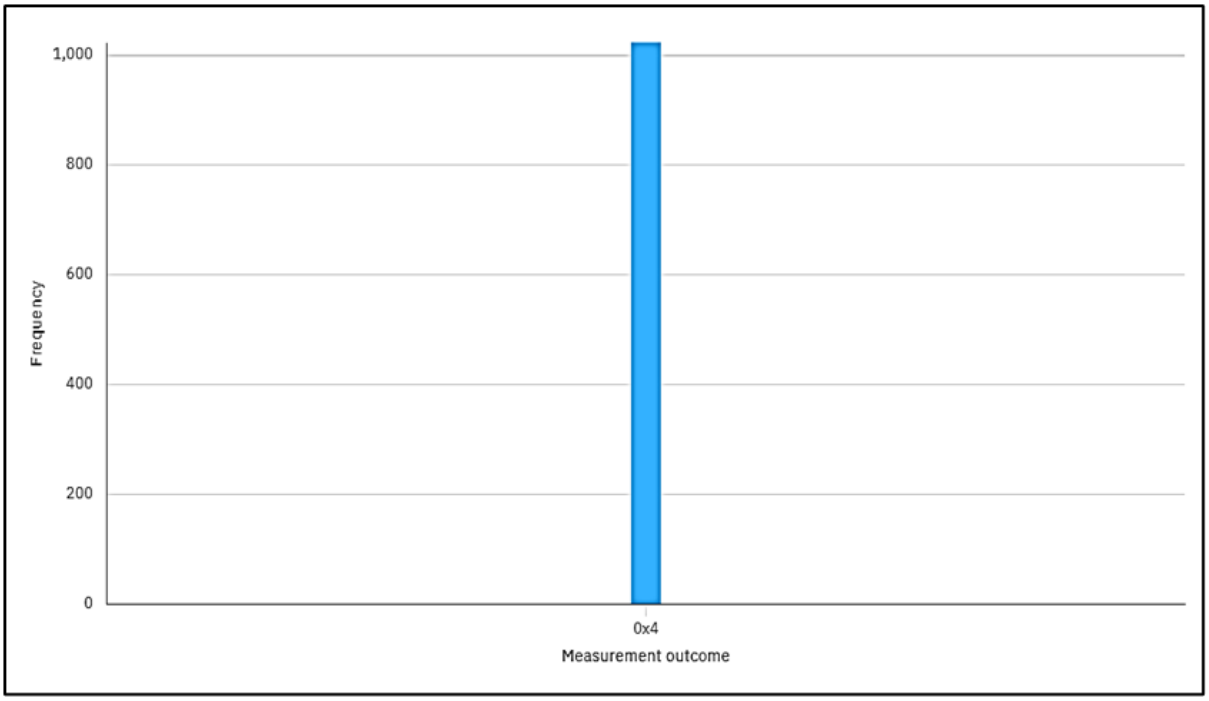

Figure 12.Output of Quantum Fault-Tolerant Reversible Adder (FTRA) – Fault

Masking Technique (TMR)

On simulating quantum FTRA including fault masking, detecting and locating mechanism using IBMQ simulator, the measurement outcome is depicted in Fig. 13. as 0x8004 which is equivalent to 00000010000000000000100 where the first and second bits from right correspond to fault check lines of Sum and Carry outputs respectively. The high value of third bit from right corresponds to garbage output B⊕C indicating that the fault is with the carry output of third module (Input C is faulty). Thus, not only is the correct output generated, masking the faulty output, but also the occurrence of a fault is detected and located, making the system design more reliable.

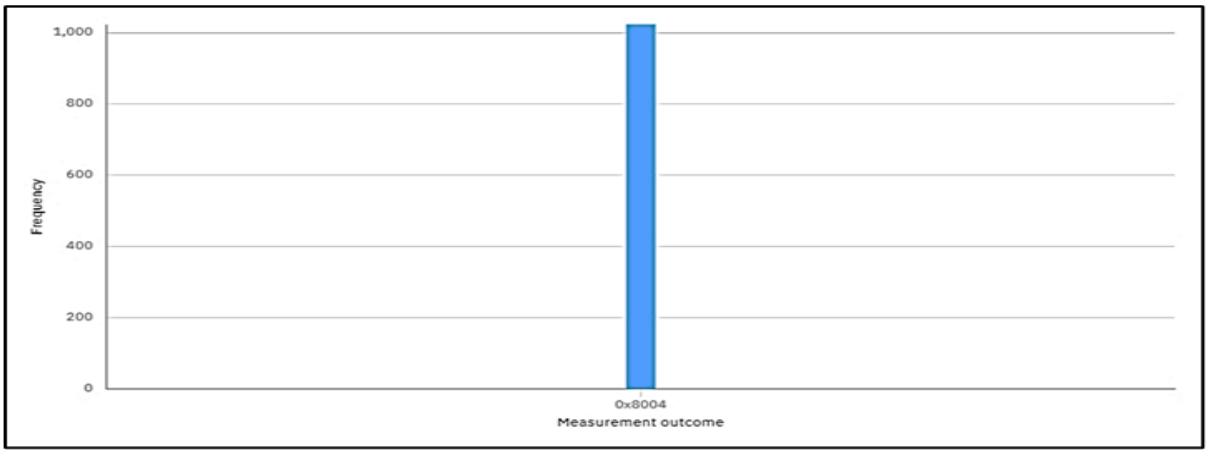

Figure 13. Output of Quantum FTRA including Fault Masking, Detecting and Locating Mechanism

Conclusion

The presented research work demonstrates a Quantum adder and subtractor circuit with Fault Tolerant Reversible Architecture combining fault masking, detection and localization mechanisms using IBM quantum composer. The proposed design is made of parity-preserving reversible gates while parity preservation alone is not sufficient for a system to be fault tolerant. The requirements for fault tolerance in quantum circuits as well as ways for achieving them are discussed. A conventional approach of triple modular redundancy will mask the effect of faulty components instantaneously leading to less probability of occurrence of faults. Being the key component of ALU design, FTRA is chosen to incorporate techniques to achieve actual fault tolerance. FTRA is employed with a 3-bit majority voter quantum circuit based on the triple modular redundancy approach and found to be effective in masking the occurrence of fault. In addition to the fault masking technique, further designs to diagnose the occurrence of fault and the location of fault in the FTRA circuit were presented and verified on simulating using IBM Quantum Simulator.

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